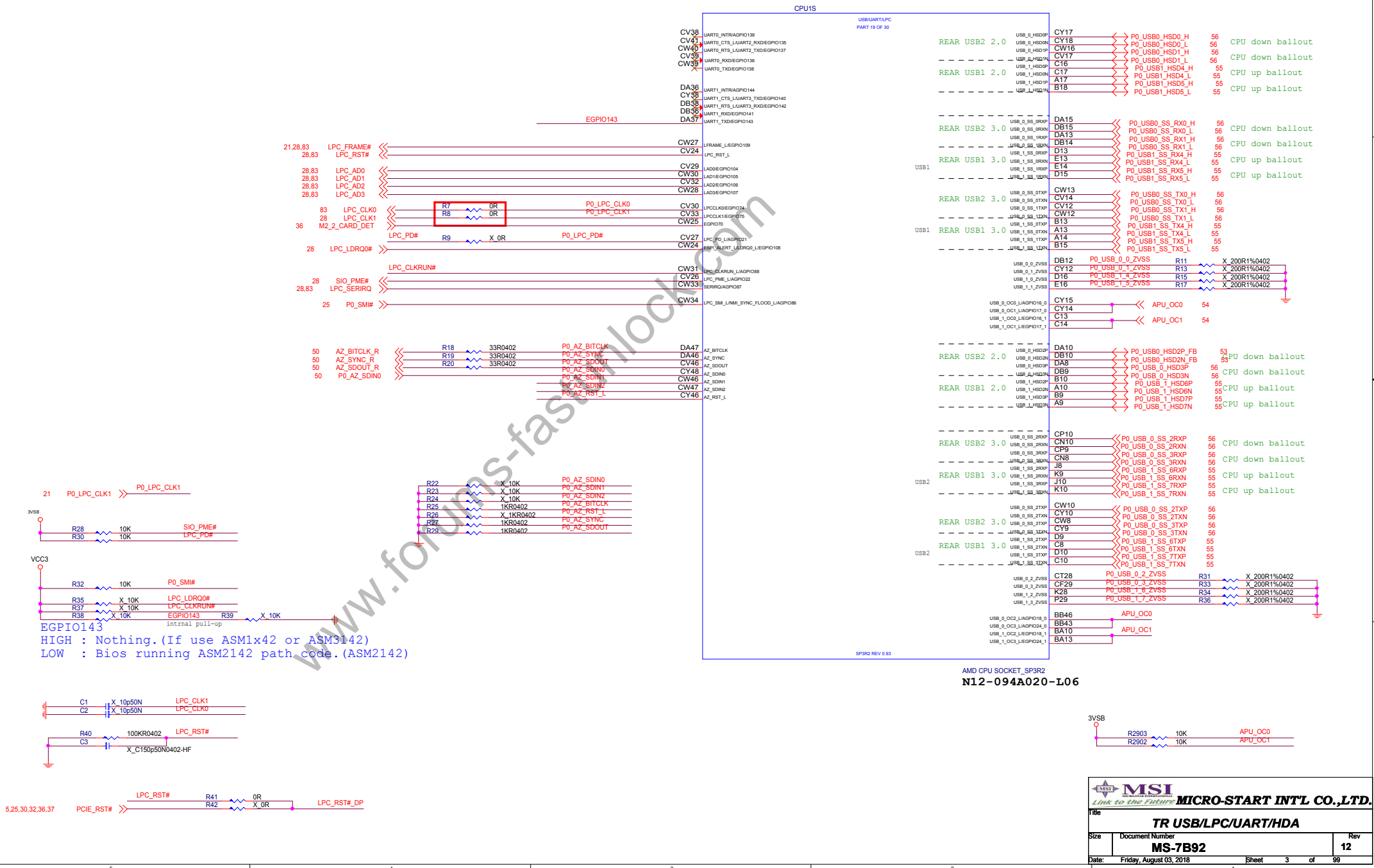


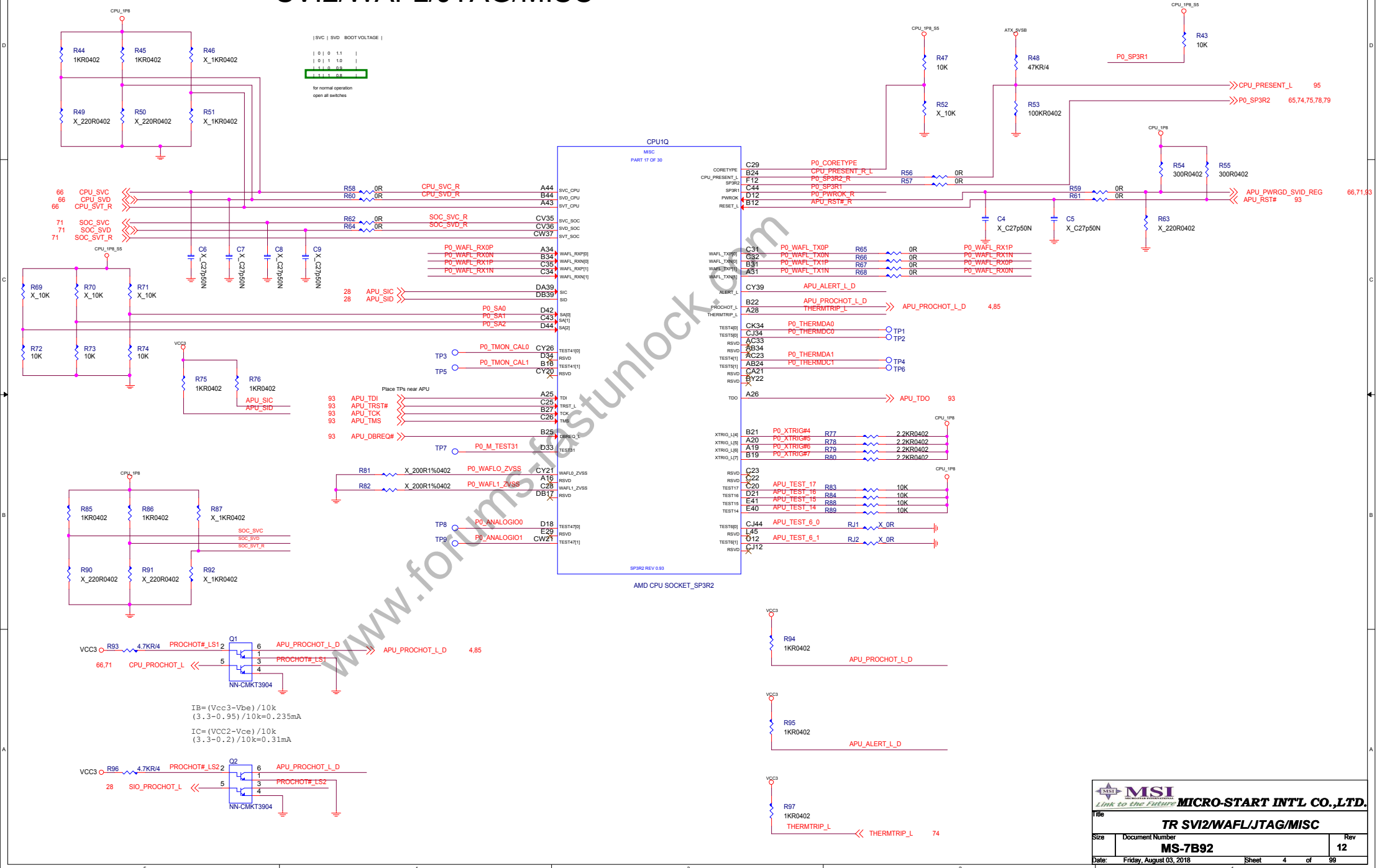
AMD TR4(X399)

Promontry X370

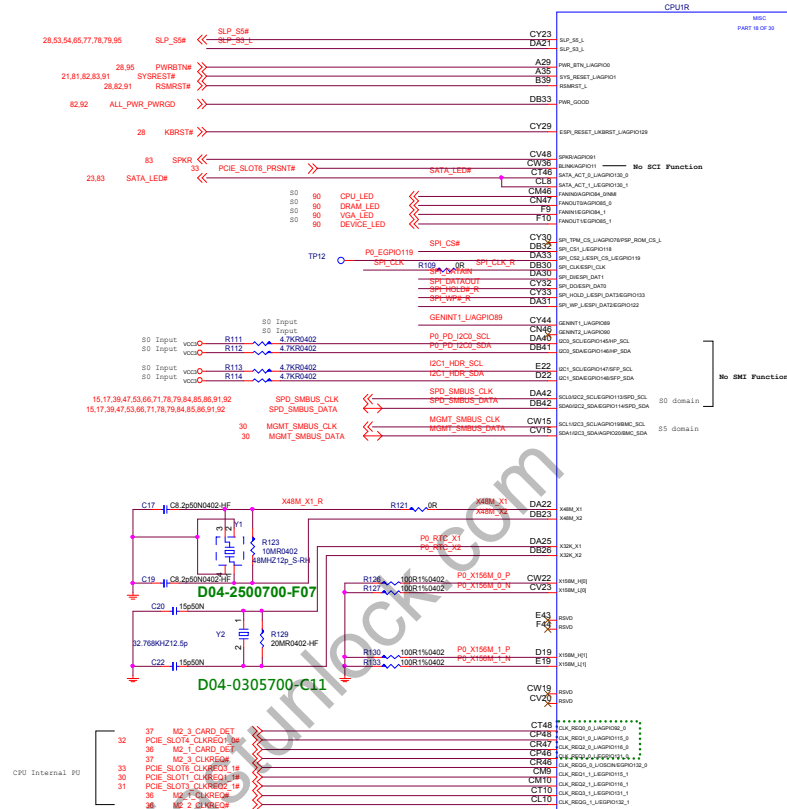
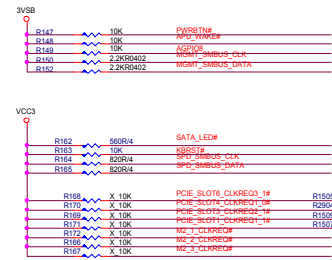
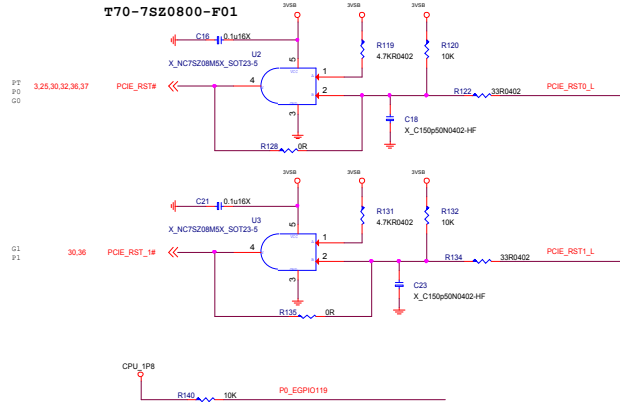
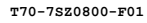
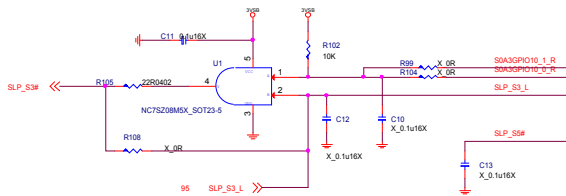
01 Cover Sheet	27 Promontory GND	65 ACPI uPI-5VDIMM&3VSB
02 Block Diagram	28 SIO NCT6797D	66~70 CPU Power IR35201 16Phase
03 SP3 USB/LPC/UART/HDA	29 SIO HWM/PS2/Debug LED	71/72 CPU Power SOC IR35204 2Phase
04 SP3 SVI2/WAFL/JTAG/MISC	30 PCIE X16 Slot1	73 CPU Power VDDCR_SOC_S5
05 SP3 ACPI/SPI/I2C/CLK/GPIO	31 PCIE X8 Slot3	74 CPU Power Connector/RT9553B
06 SP3 PCIE	32 PCIE X16 Slot4	75 CPU Power 1P8V-MP2147
07 SP3 MEMORY A	33 PCIE X8 Slot5	76 CPU Power Audio-GS7133
08 SP3 MEMORY B	34 PCIE X1 Slot2	77 DDR PWR VPP25-MP2145/VTT
09 SP3 MEMORY C	35 SATA Connector	78/79 DDR01/02 PV4210-2 phase
10 SP3 MEMORY D	36/37 M2_1/M2_2/M2_3 Connector	80 VTTDDR
11 SP3 POWER	38 M2_4 WIFI+BT	81 PM-SY8288 1.05V/GS7133-2.5V
12 SP3 Reserved	39 NCT5635Y FAN NCT7718 Temp	82 CPU Power Good
13 SP3 DECOUPLING Cap	40 CPU FAN1-TYPE J	83 ATX/Front Panel
14 SP3 GND	41 CPU FAN2-TYPE K(PUMP)	84 RTC/Clear CMOS Circuit
15 DDR4 - DIMM_A	42/43/44 SYSTEM FAN1/2/3/4/5-TYPE K	85 OV Control/NCT3933/NCT5635Y
16 DDR4 - DIMM_B	45/46/47 EXTFAN1/2/3-NCT7802 IC	86/87 LED MCU Control JRGB/JCORSAIR/JRAINBOW
17 DDR4 - DIMM_C	48/49 LAN1/LAN2-Intel I211AT	88 LED BOARD SIDE
18 DDR4 - DIMM_D	50/52 Audio ALC1220P-48PIN	90 LED DIMM/Debug
19 DDR4 - POWER	53 USB2.0 Flash BIOS F75504	91/92 Clock Gen Clock Buffer
20 DDR4 - GND	54 USB Power	93 APU_HDT_DEBUG
21 CPU STRAPS	55/56 USB3.0 Rear Side	94 BOM Option
22 Promontory USB	57/58 Pericom1004 Redriver Rear Side-TYPE-C	95 EMI CAP/ SLG IC
23 Promontory PCIE/SATA	59/60 USB3.1 ASM3142	
24 Promontory CLOCK	61 USB2.0 Front Side-JUSB1/2	
25 Promontory GPIO/SMB/SPI	62 USB3.0 Front Side-JUSB4	
26 Promontory POWER	63/64 USB3.0 Front Side-JUSB5(Charge port)	

USB/LPC/UART/HDA

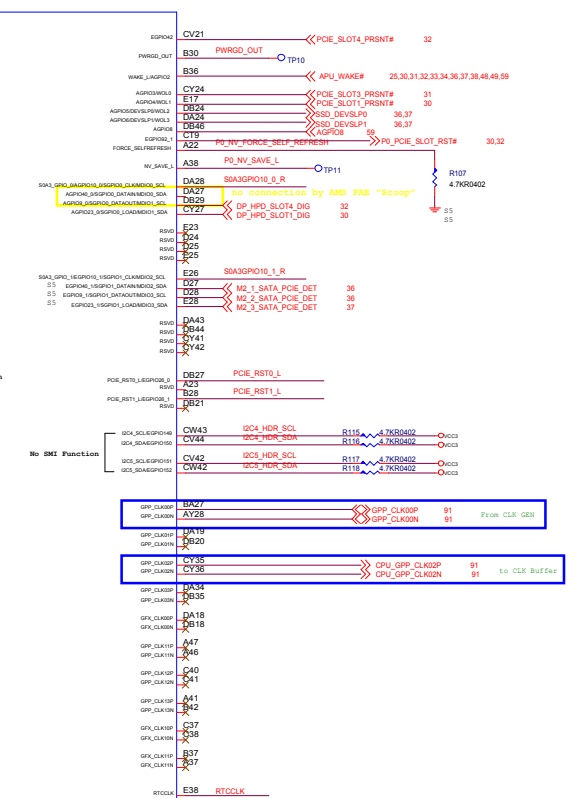
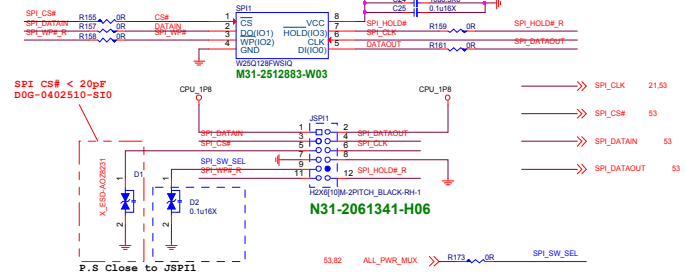




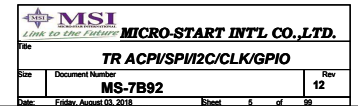
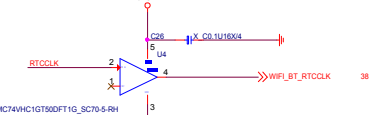
ACPI/SPI/I2C/CLK/GPIO

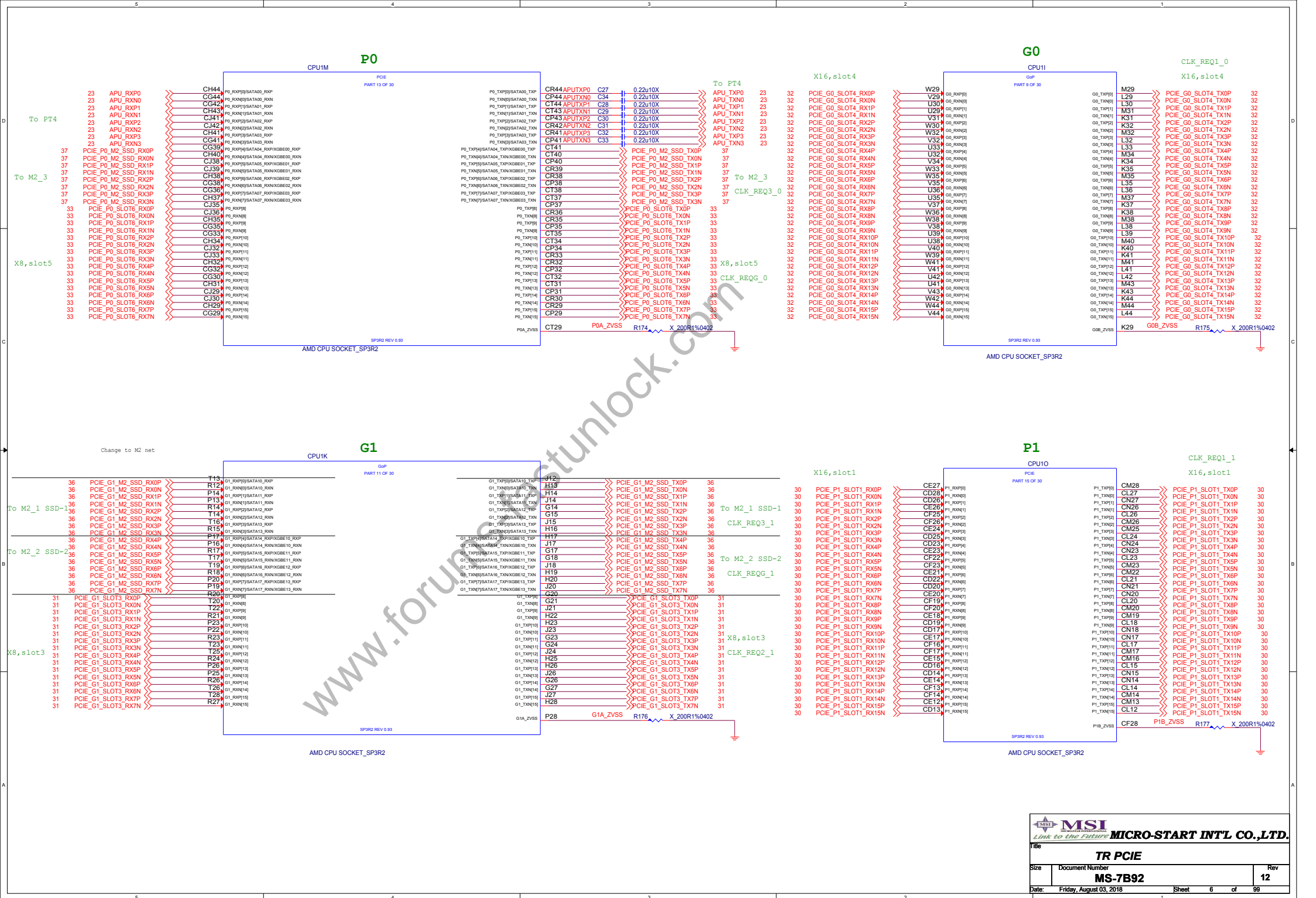


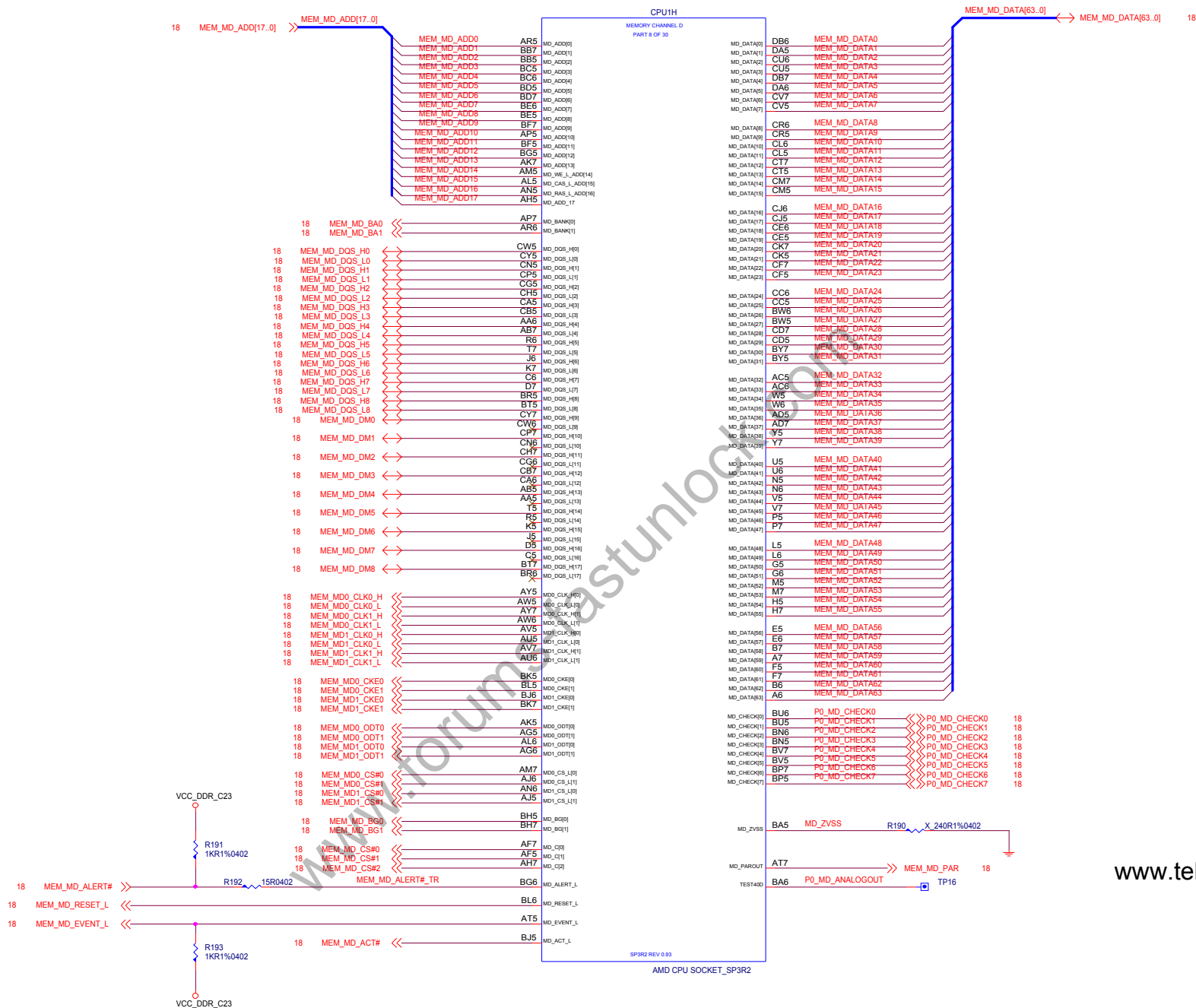
SPI ROM (1.8V)



N12-094A020-L06

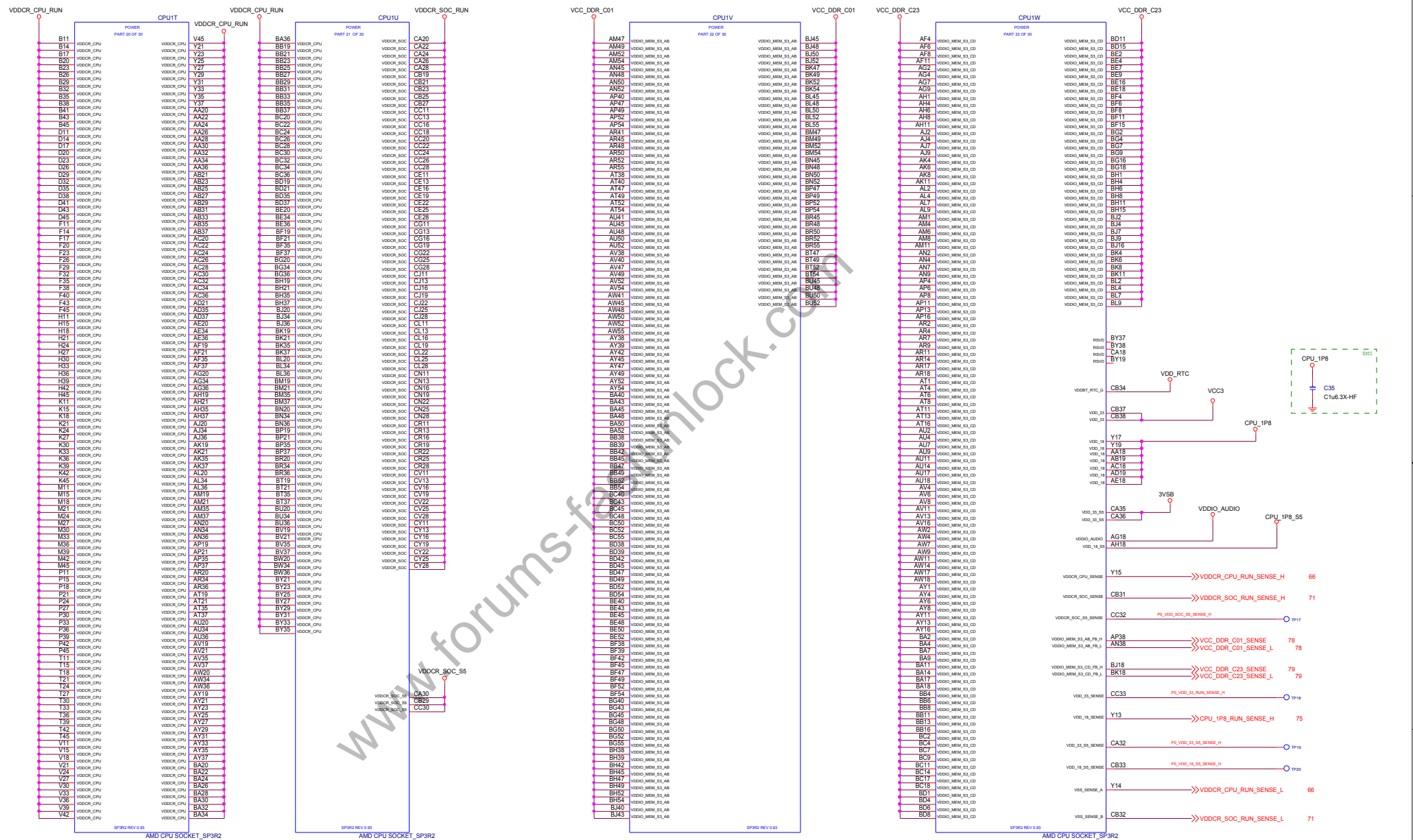


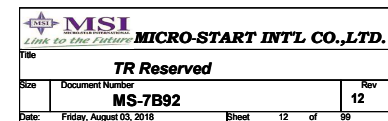




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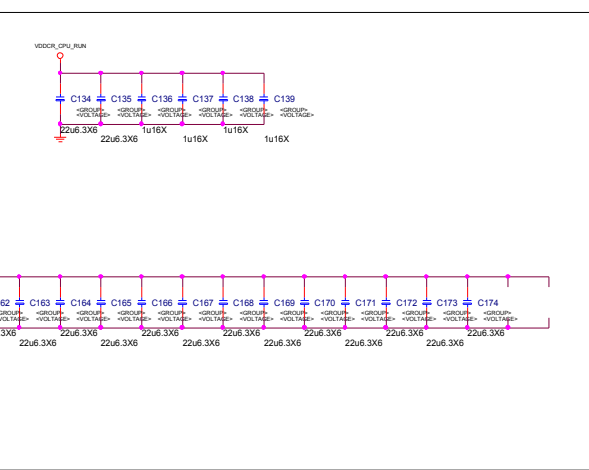
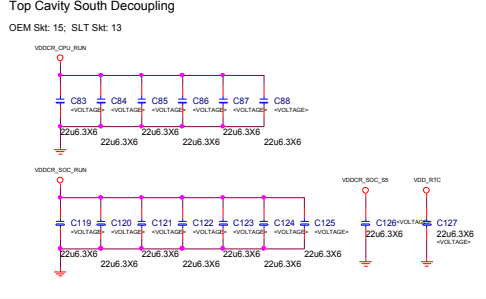
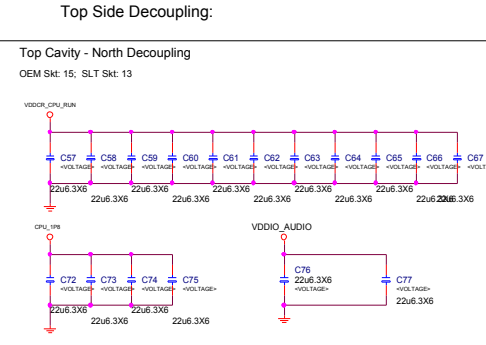
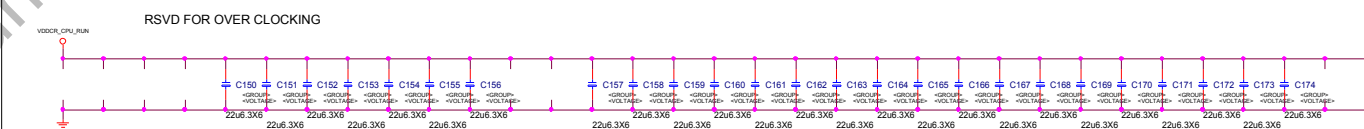
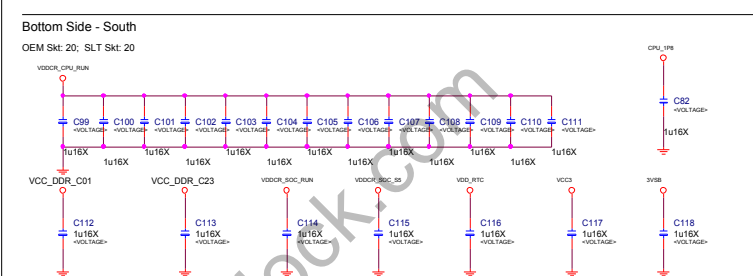
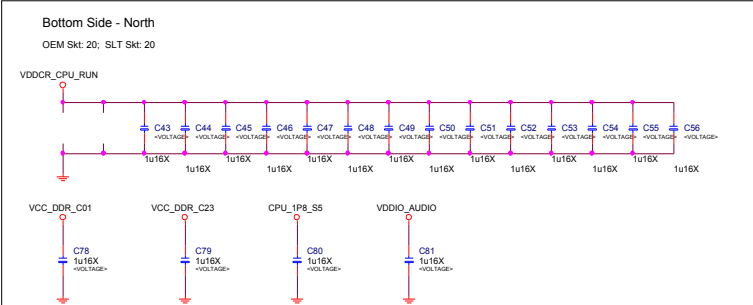
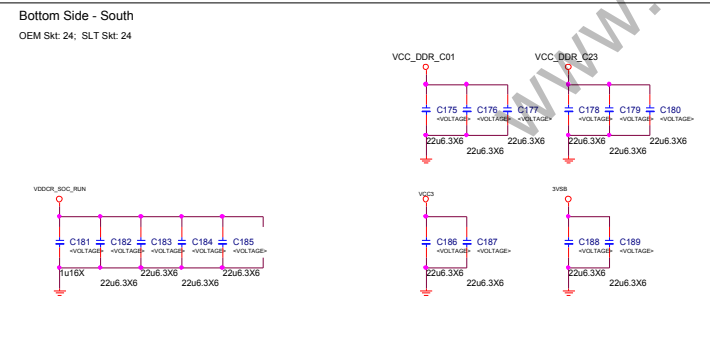
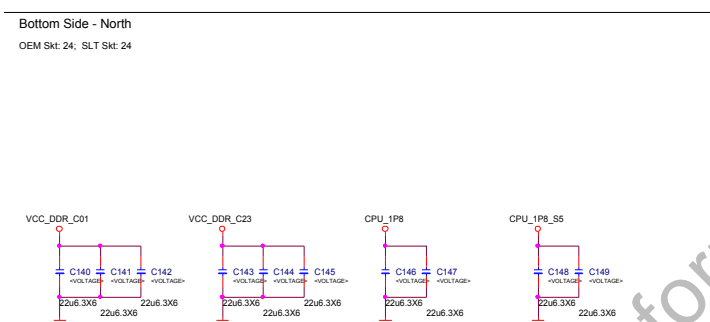
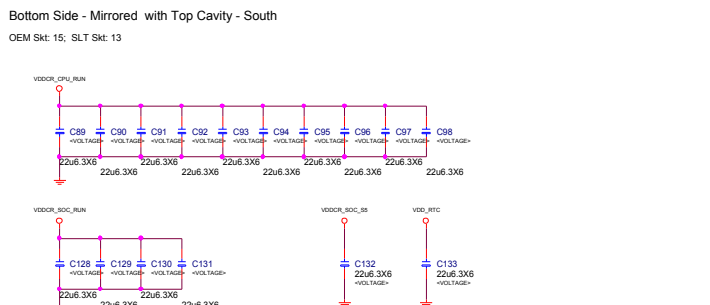
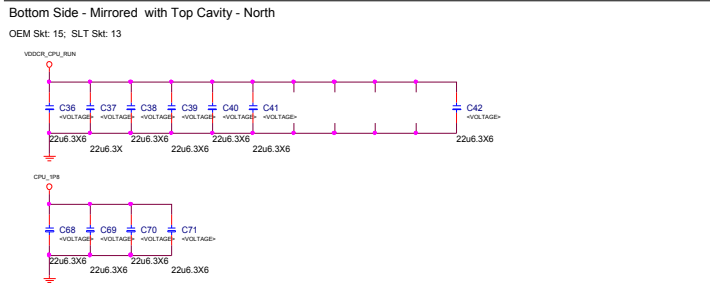
POWER



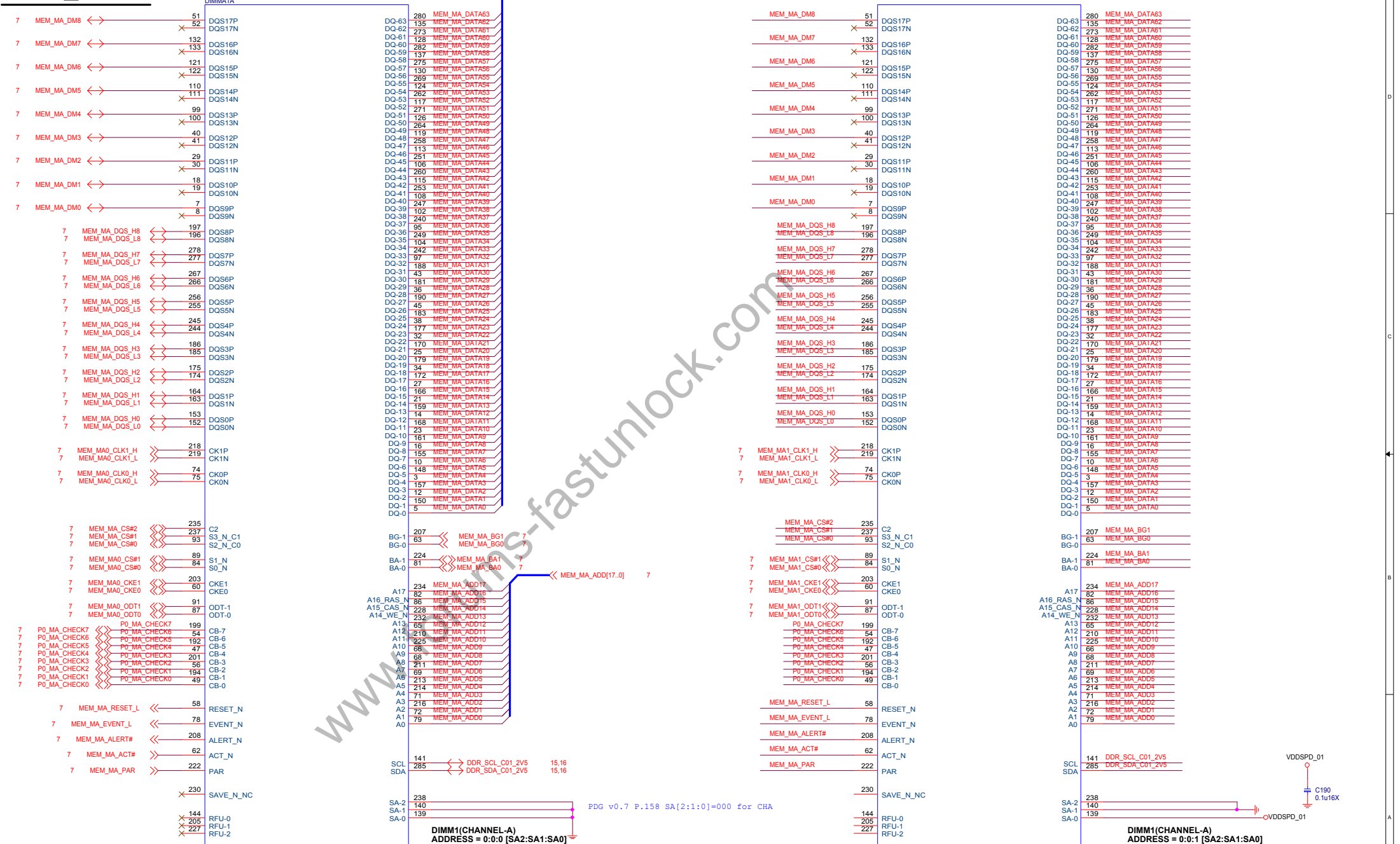


Decoupling Grouped by Placement Location

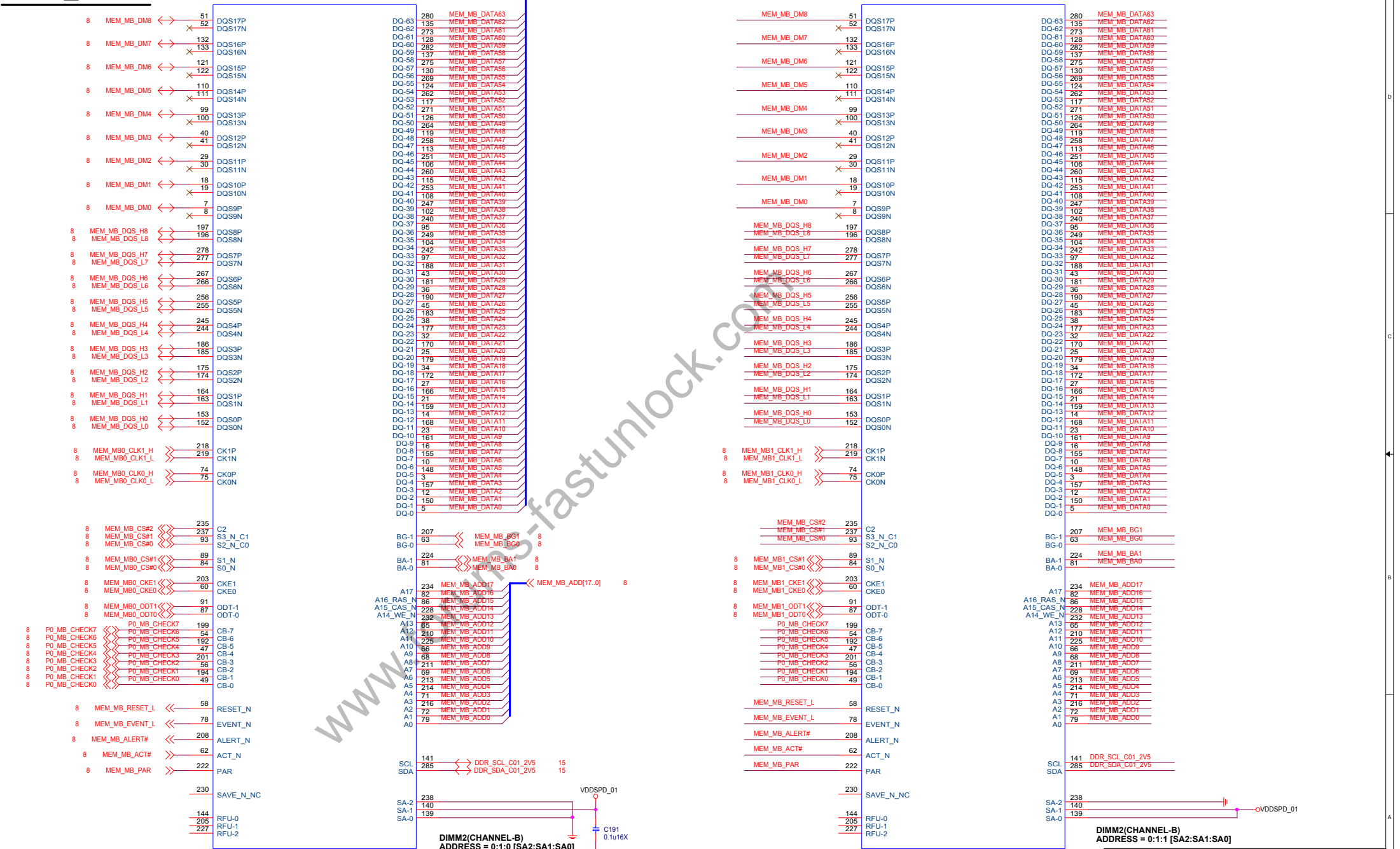
VDDCR_CPU Bottom Side Decoupling:



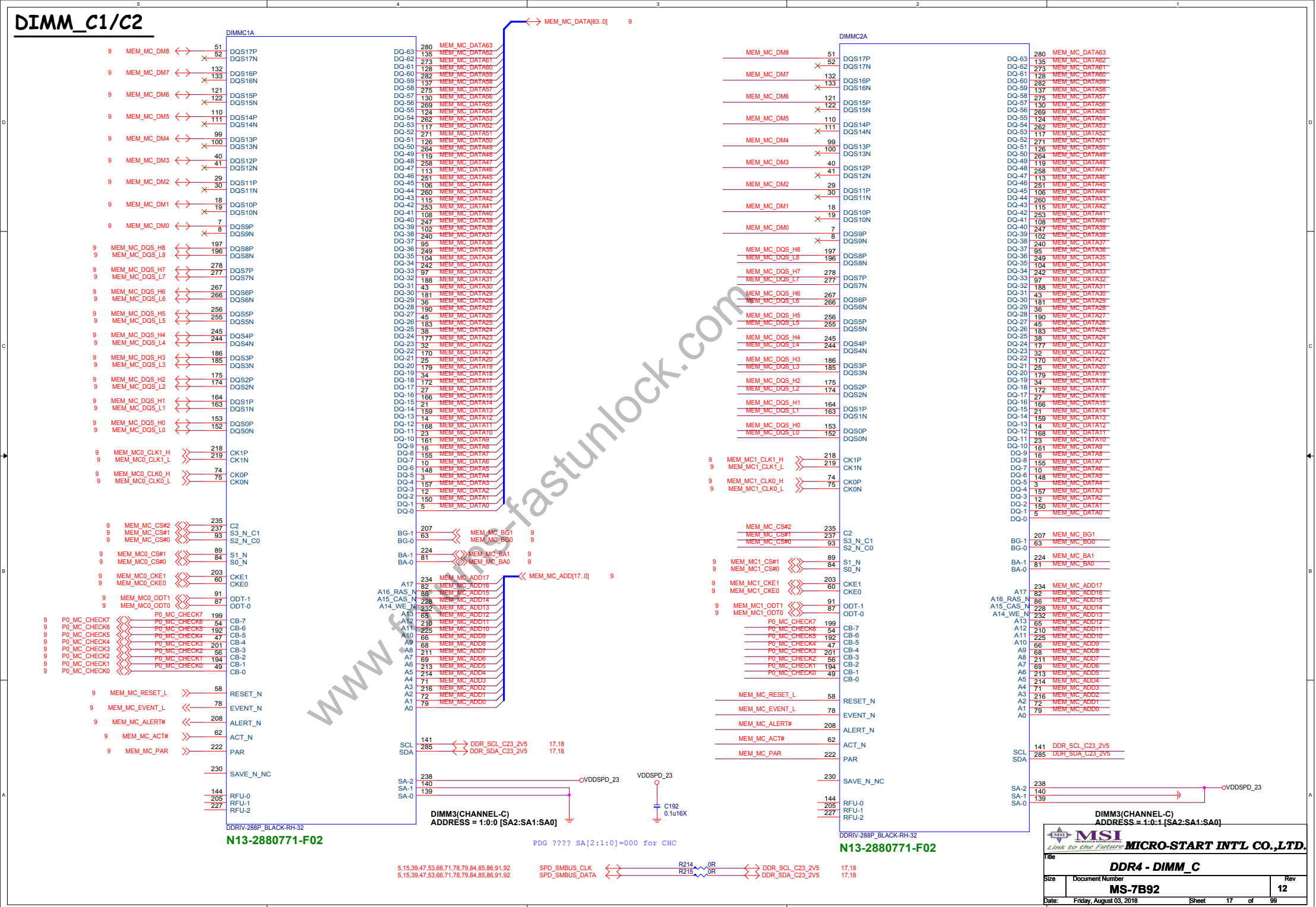
DIMM_A1/A2



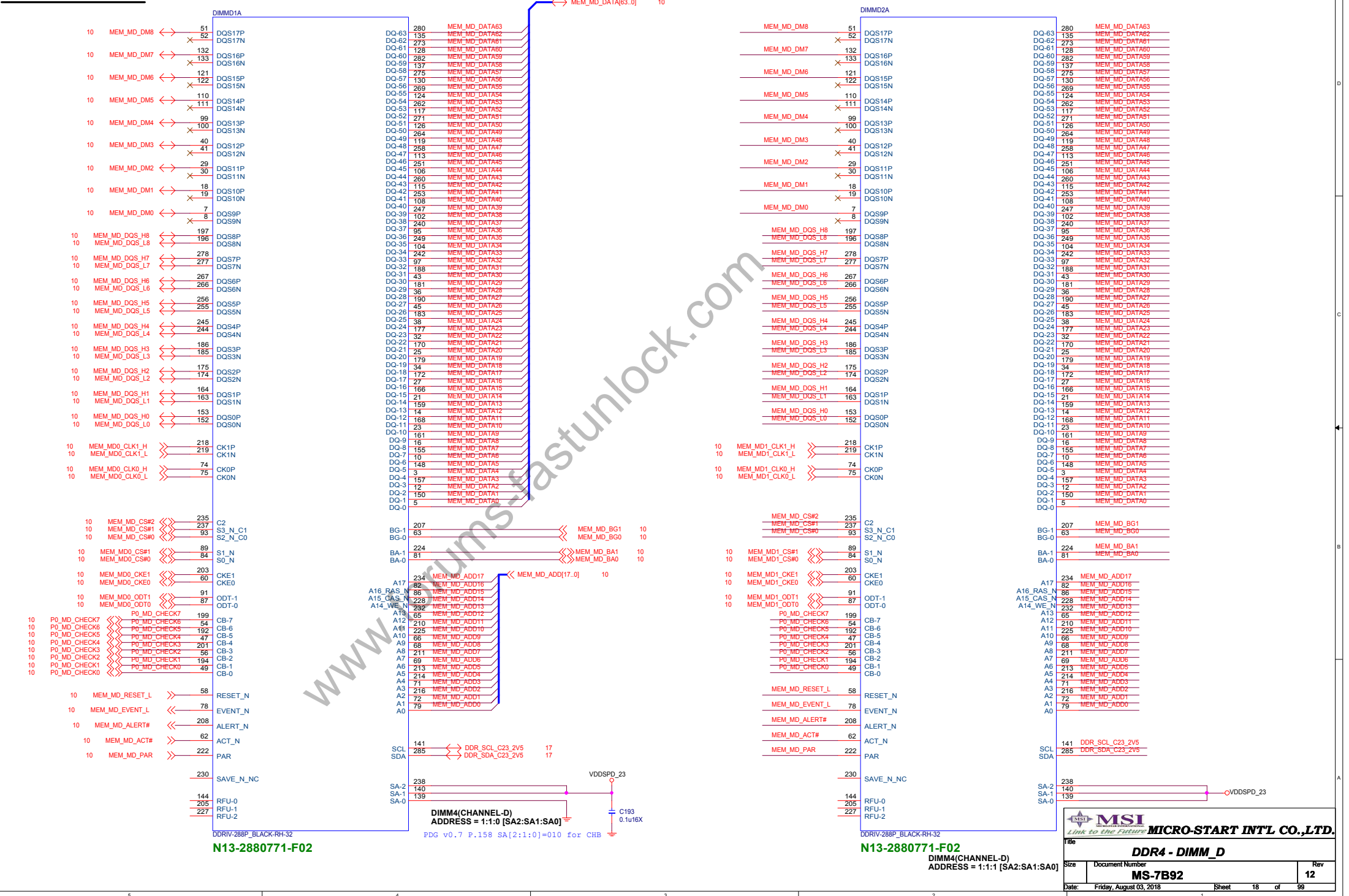
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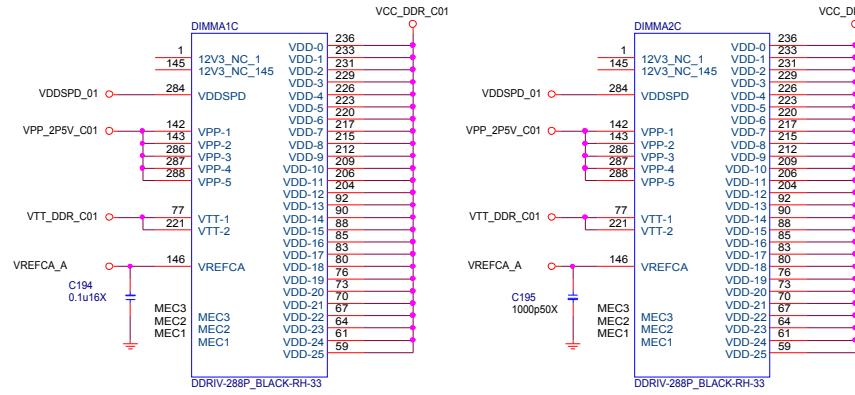


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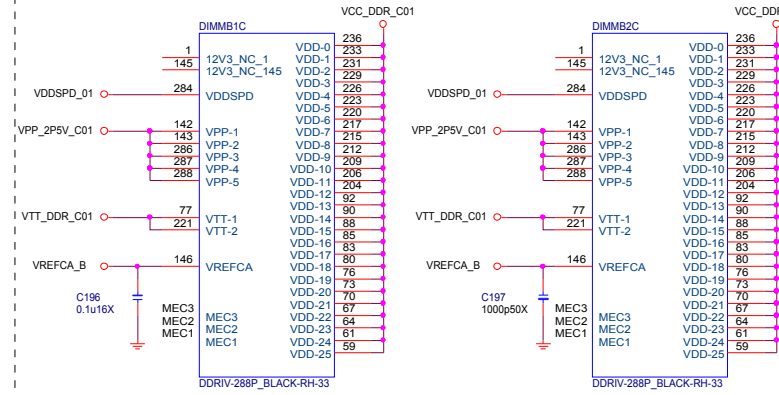
DIMM_D1/D2





N13-2880811-F02

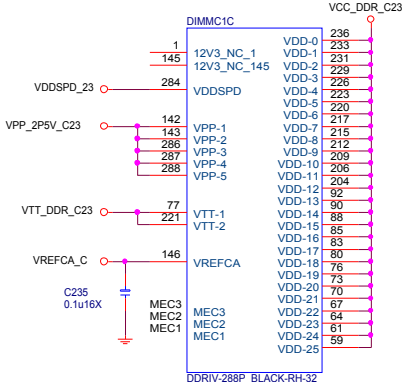
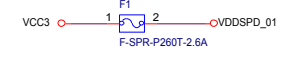
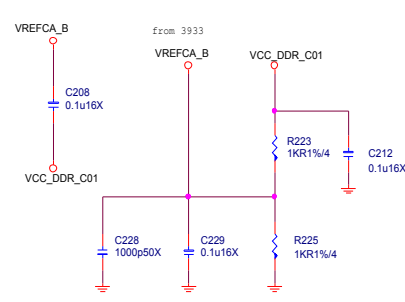
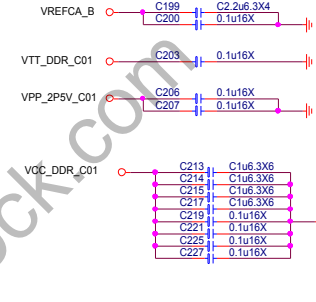
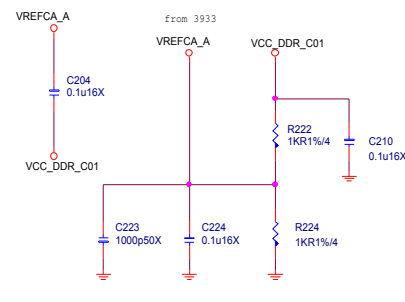
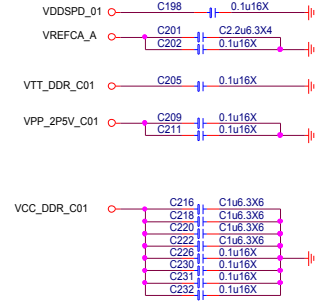
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N13-2880811-F02

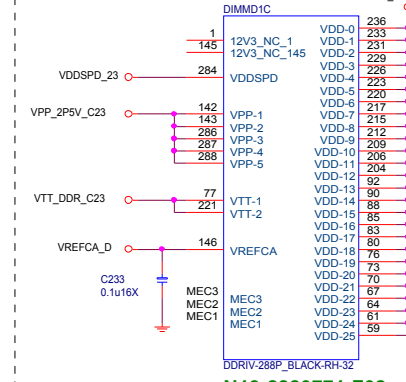
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DDR VREF
(place resistors close to DIMMs)



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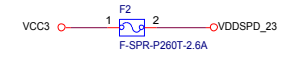
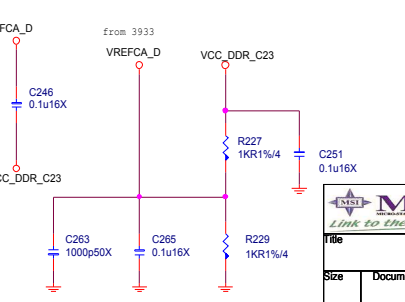
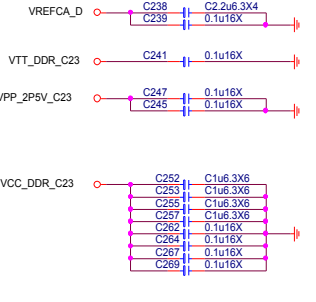
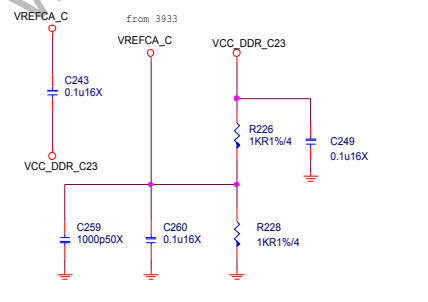
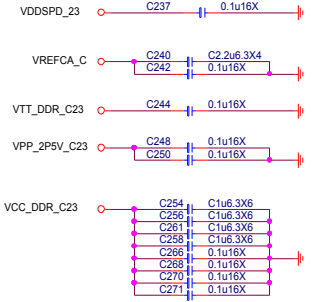
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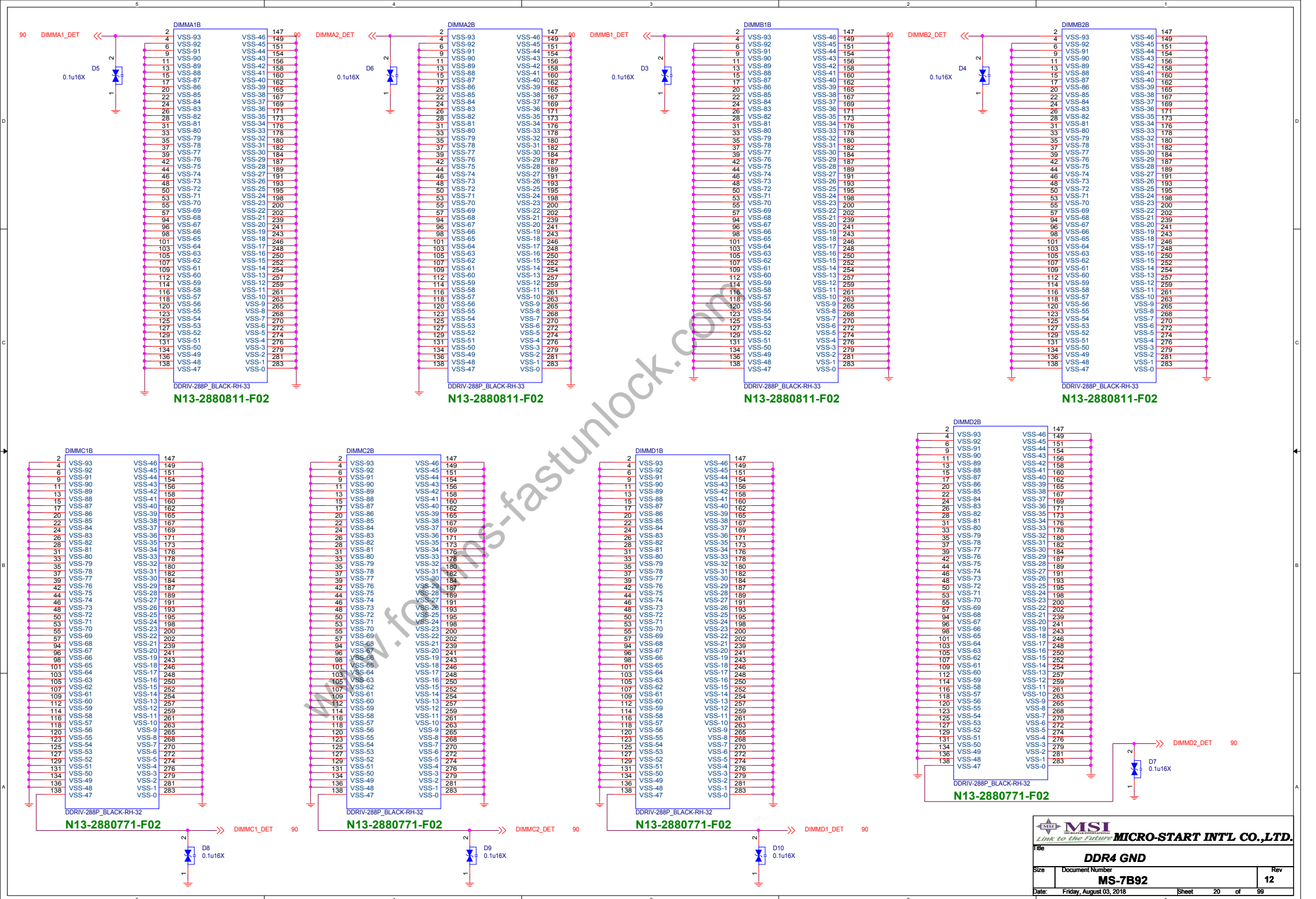
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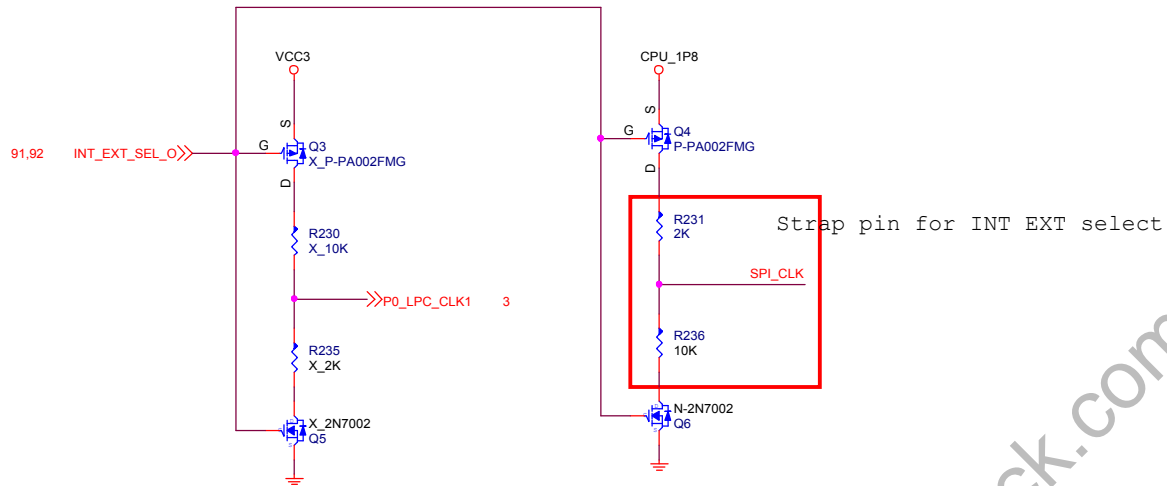
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DDR VREF
(place resistors close to DIMMs)



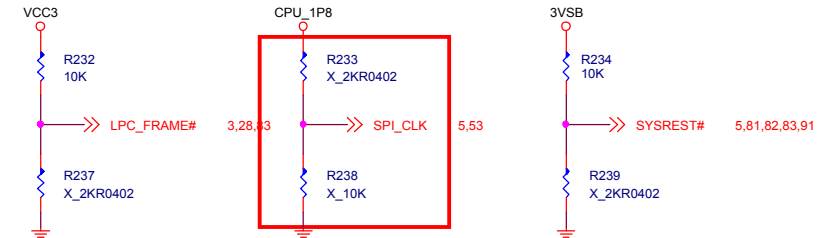
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Size	Document Number	Rev
	MS-7B92	12
Date:	Friday, August 03, 2018	Sheet 19 of 99



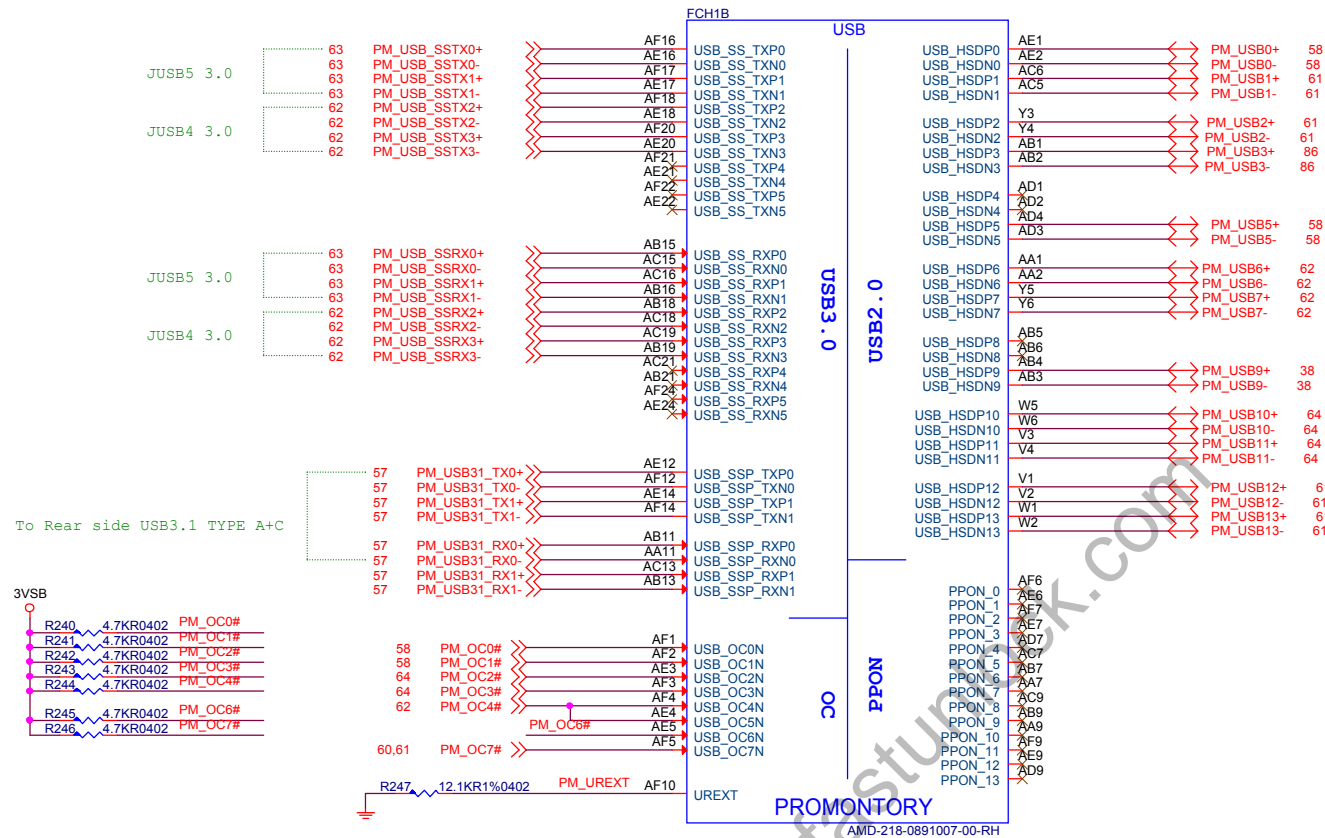


CPU STRAPS

STRAP	DEFINITION
SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RST#	1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE
LPC_FRAME_L	ROM TYPE SELECT 1:BOOT FROM SPI ROM(DEFAULT) 0:BOOT FROM LPC ROM



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Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SS_TX/RXP[N]0	USB_HSDP[N]5	USB_OC0N
USB_SS_TX/RXP[N]1	USB_HSDP[N]0	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP[N]0	USB_HSDP[N]10	USB_OC2N
USB_SS_TX/RXP[N]1	USB_HSDP[N]11	USB_OC3N
USB_SS_TX/RXP[N]2	USB_HSDP[N]6	USB_OC4N
USB_SS_TX/RXP[N]3	USB_HSDP[N]7	USB_OC5N
USB_SS_TX/RXP[N]4	USB_HSDP[N]8	USB_OC6N
USB_SS_TX/RXP[N]5	USB_HSDP[N]9	USB_OC7N
	USB_HSDP[N]1	USB_OC7N
	USB_HSDP[N]2	USB_OC7N
	USB_HSDP[N]3	USB_OC7N
	USB_HSDP[N]4	USB_OC7N
	USB_HSDP[N]12	USB_OC7N
	USB_HSDP[N]13	USB_OC7N

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

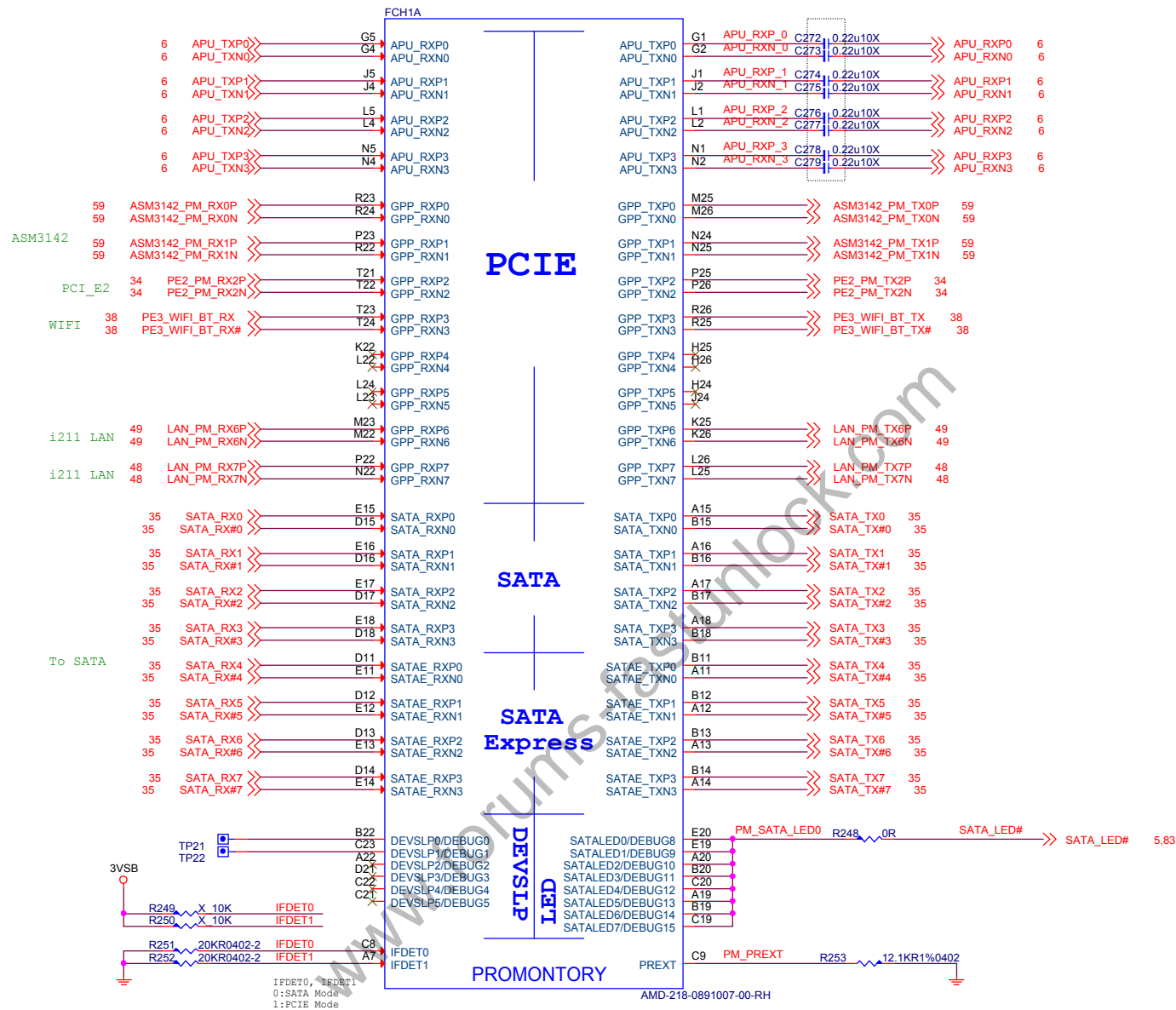
CLK2.3不能用
CLK1-3不能用于

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Title: **Promontory USB**

Size: Document Number **MS-7B92** Rev **12**

Date: Friday, August 03, 2018 Sheet 22 of 99



SATA port	DEVSLP signal
SATA_TX/RXP/N[0]	DEVSLP0
SATA_TX/RXP/N[1]	DEVSLP1
SATA_TX/RXP/N[2]	DEVSLP2
SATA_TX/RXP/N[3]	DEVSLP3
SATAE_TX/RXP/N[0]	SATAE_CLKREQ0N
SATAE_TX/RXP/N[1]	DEVSLP4
SATAE_TX/RXP/N[2]	SATAE_CLKREQ1N
SATAE_TX/RXP/N[3]	DEVSLP5

MSI

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Link to the future

Title

Promontory PCIE/SATA

Size

Document Number

MS-7B92

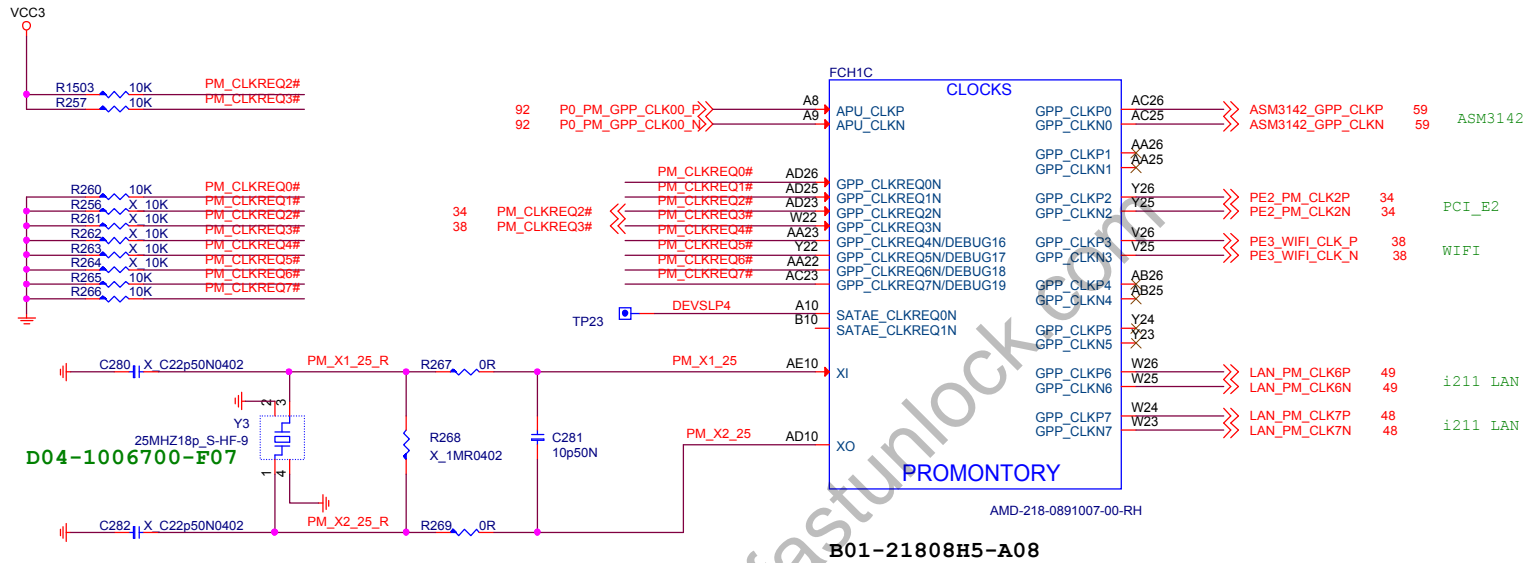
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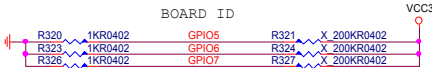
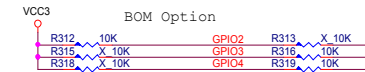
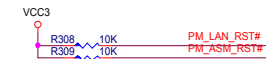
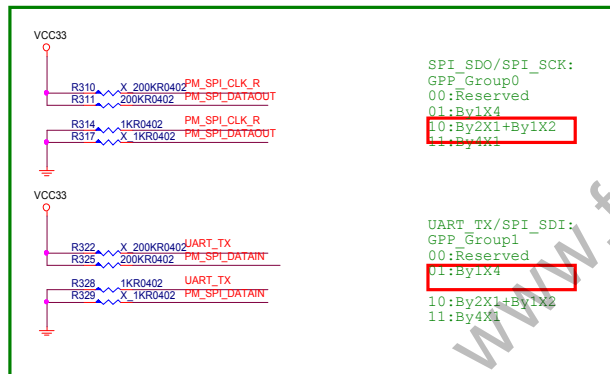
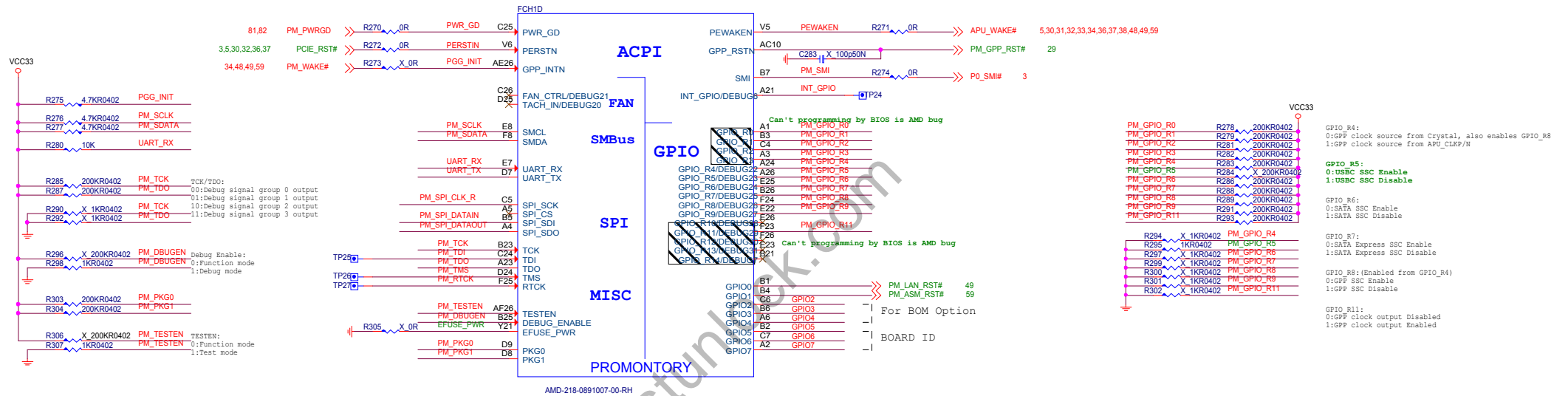
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Sheet 23 of 99

Rev

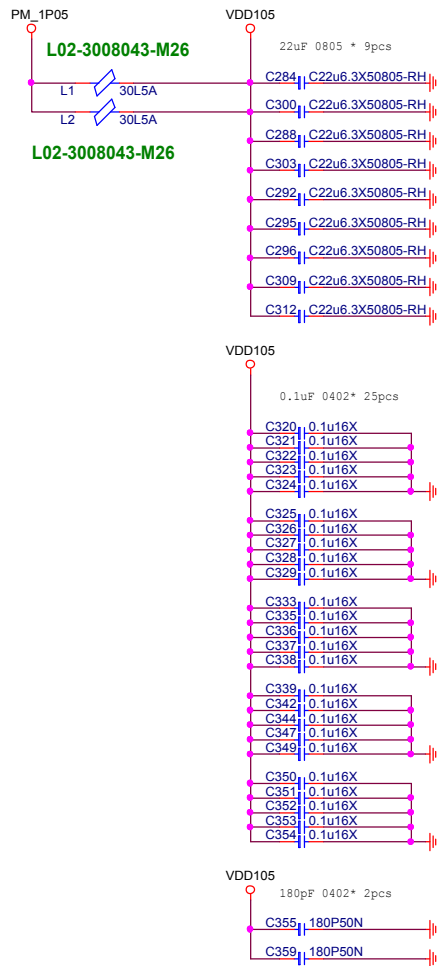
12





GPIO2=0 --> SLG41837
Slave Address:PCB1.0 version
00110000 , Wite , 30
00110001 , Read , 31

GPIO2=1 --> SLG41837
Slave Address:PCB1.1 version
01010000 , Wite , 50
01010001 , Read , 51



5.5A

VDD105

FCH1E

H15

H17

J11

K8

K9

K13

K14

K17

L8

L17

M17

N17

P7

P8

P17

R1

R2

R3

R4

R5

R6

R7

R8

R17

T1

T2

T3

T4

T5

T6

T7

T8

T17

U1

U2

U3

U4

U5

U6

U7

U8

U17

V9

V10

V11

V14

V15

V16

V20

V21

W11

W13

W16

VDD105_0

VDD105_1

VDD105_2

VDD105_3

VDD105_4

VDD105_5

VDD105_6

VDD105_7

VDD105_8

VDD105_9

VDD105_10

VDD105_11

VDD105_12

VDD105_13

VDD105_14

VDD105_15

VDD105_16

VDD105_17

VDD105_18

VDD105_19

VDD105_20

VDD105_21

VDD105_22

VDD105_23

VDD105_24

VDD105_25

VDD105_26

VDD105_27

VDD105_28

VDD105_29

VDD105_30

VDD105_31

VDD105_32

VDD105_33

VDD105_34

VDD105_35

VDD105_36

VDD105_37

VDD105_38

VDD105_39

VDD105_40

VDD105_41

VDD105_42

VDD105_43

VDD105_44

VDD105_45

VDD105_46

VDD105_47

VDD105_48

VDD105_49

VDD105_50

VDD105_51

VDD105_52

POWER

PROMONTORY

AMD-218-0891007-00-RH

900mA

VCC25

C1

C2

C3

D1

D2

D3

D4

D5

D6

E1

E2

E3

E4

E5

E6

F6

K11

K12

K15

K16

M8

M19

N8

N19

P19

R19

V12

V13

V17

VCC25_0

VCC25_1

VCC25_2

VCC25_3

VCC25_4

VCC25_5

VCC25_6

VCC25_7

VCC25_8

VCC25_9

VCC25_10

VCC25_11

VCC25_12

VCC25_13

VCC25_14

VCC25_15

VCC25_16

VCC25_17

VCC25_18

VCC25_19

VCC25_20

VCC25_21

VCC25_22

VCC25_23

VCC25_24

VCC25_25

VCC25_26

VCC25_27

VCC25_28

VCC25_29

VCC25_30

VCC25_31

VCC25_32

VCC25_33

VCC25_34

VCC25_35

VCC25_36

VCC25_37

VCC25_38

VCC25_39

VCC25_40

VCC25_41

VCC25_42

VCC25_43

VCC25_44

VCC25_45

VCC25_46

VCC25_47

VCC25_48

VCC25_49

VCC25_50

VCC25_51

VCC25_52

VCC25_53

VCC25_54

VCC25_55

VCC25_56

VCC25_57

VCC25_58

VCC25_59

VCC25_60

VCC25_61

VCC25_62

VCC25_63

VCC25_64

VCC25_65

VCC25_66

VCC25_67

VCC25_68

VCC25_69

VCC25_70

VCC25_71

VCC25_72

VCC25_73

VCC25_74

VCC25_75

VCC25_76

VCC25_77

VCC25_78

VCC25_79

VCC25_80

VCC25_81

VCC25_82

VCC25_83

VCC25_84

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VCC25_92

VCC25_93

VCC25_94

VCC25_95

VCC25_96

VCC25_97

VCC25_98

VCC25_99

VCC25_100

VCC25_101

VCC25_102

VCC25_103

VCC25_104

VCC25_105

VCC25_106

VCC25_107

VCC25_108

VCC25_109

VCC25_110

VCC25_111

VCC25_112

VCC25_113

VCC25_114

VCC25_115

VCC25_116

VCC25_117

VCC25_118

VCC25_119

VCC25_120

VCC25_121

VCC25_122

VCC25_123

VCC25_124

VCC25_125

VCC25_126

VCC25_127

VCC25_128

VCC25_129

VCC25_130

VCC25_131

VCC25_132

VCC25_133

VCC25_134

VCC25_135

VCC25_136

VCC25_137

VCC25_138

VCC25_139

VCC25_140

VCC25_141

VCC25_142

VCC25_143

VCC25_144

VCC25_145

VCC25_146

VCC25_147

VCC25_148

VCC25_149

VCC25_150

VCC25_151


VCC25_152

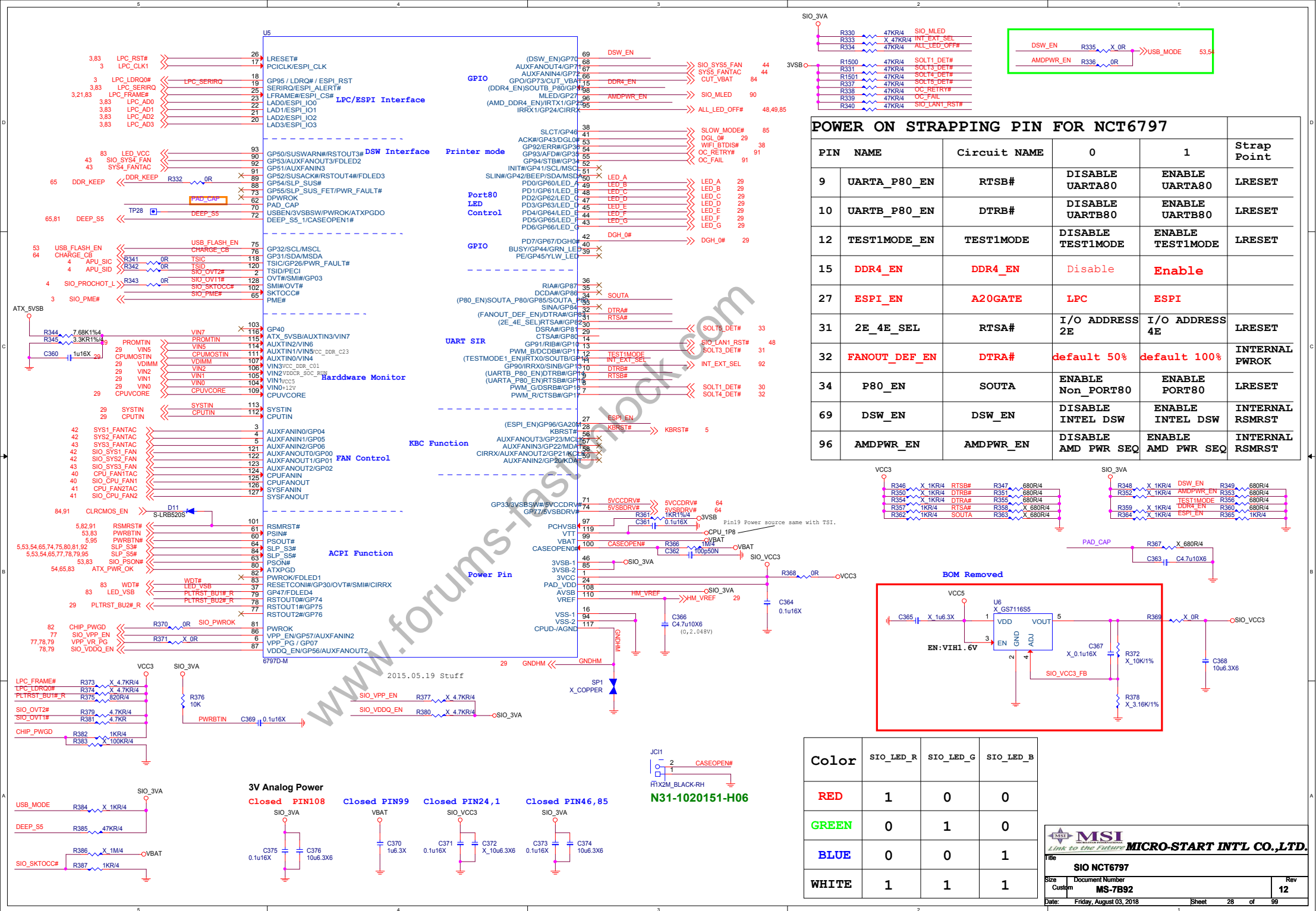
VCC25_153

GND

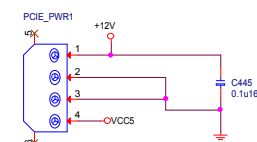
PROMONTORY

AMD-218-0891007-00-RH

 MICRO-START INT'L CO.,LTD.		
Title		
Promontory GND		
Size	Document Number	Rev
	MS-7B92	12
Date:	Friday, August 03, 2018	Sheet 27 of 99



PCI EXPRESS X16 SLOT

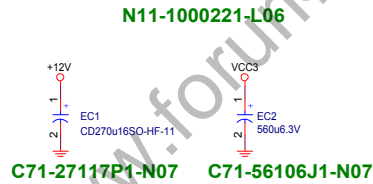
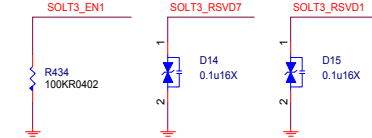
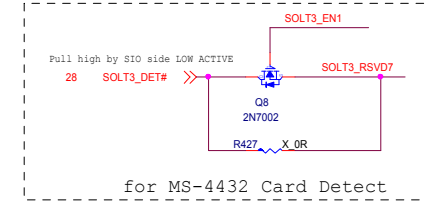
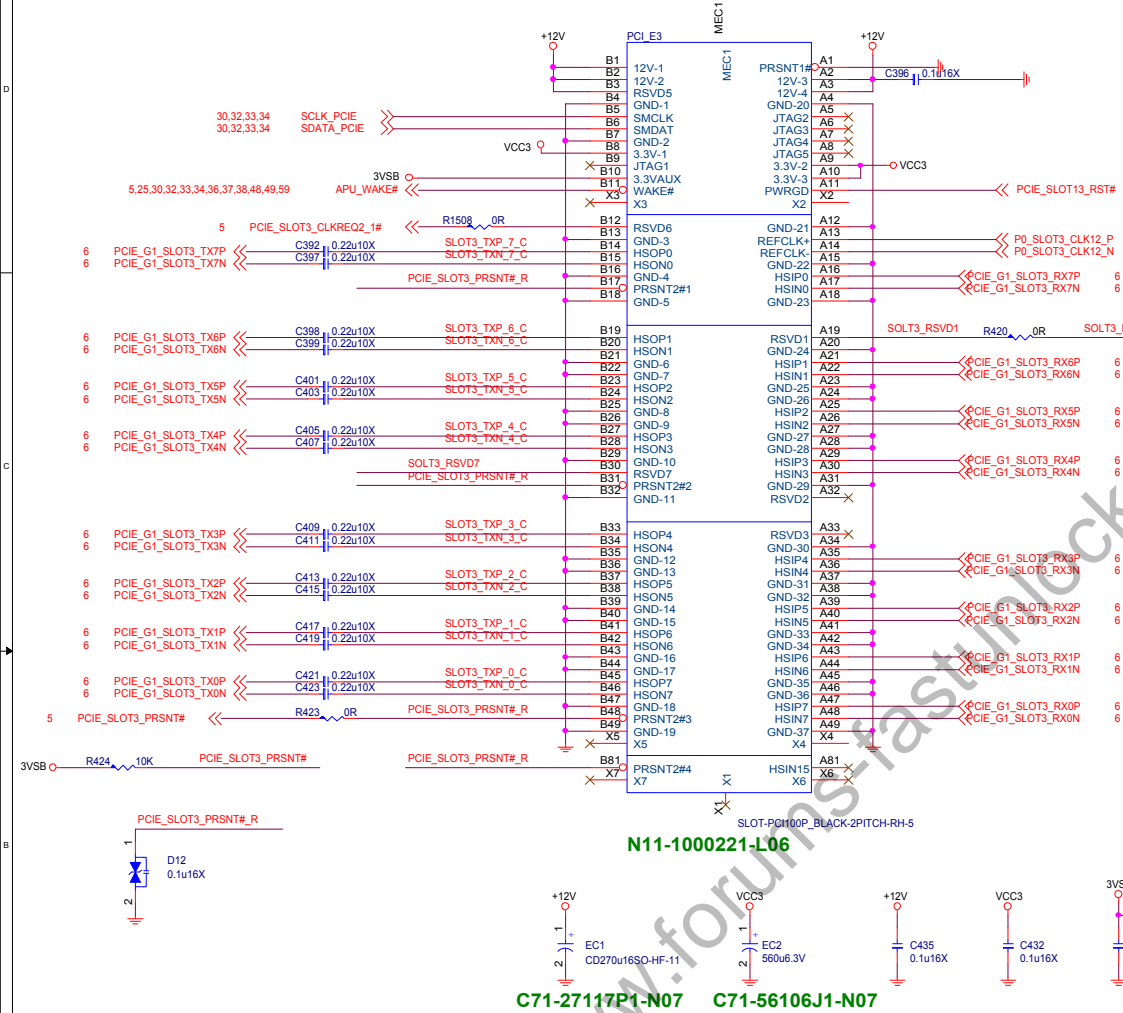


C71-27117P1-N07

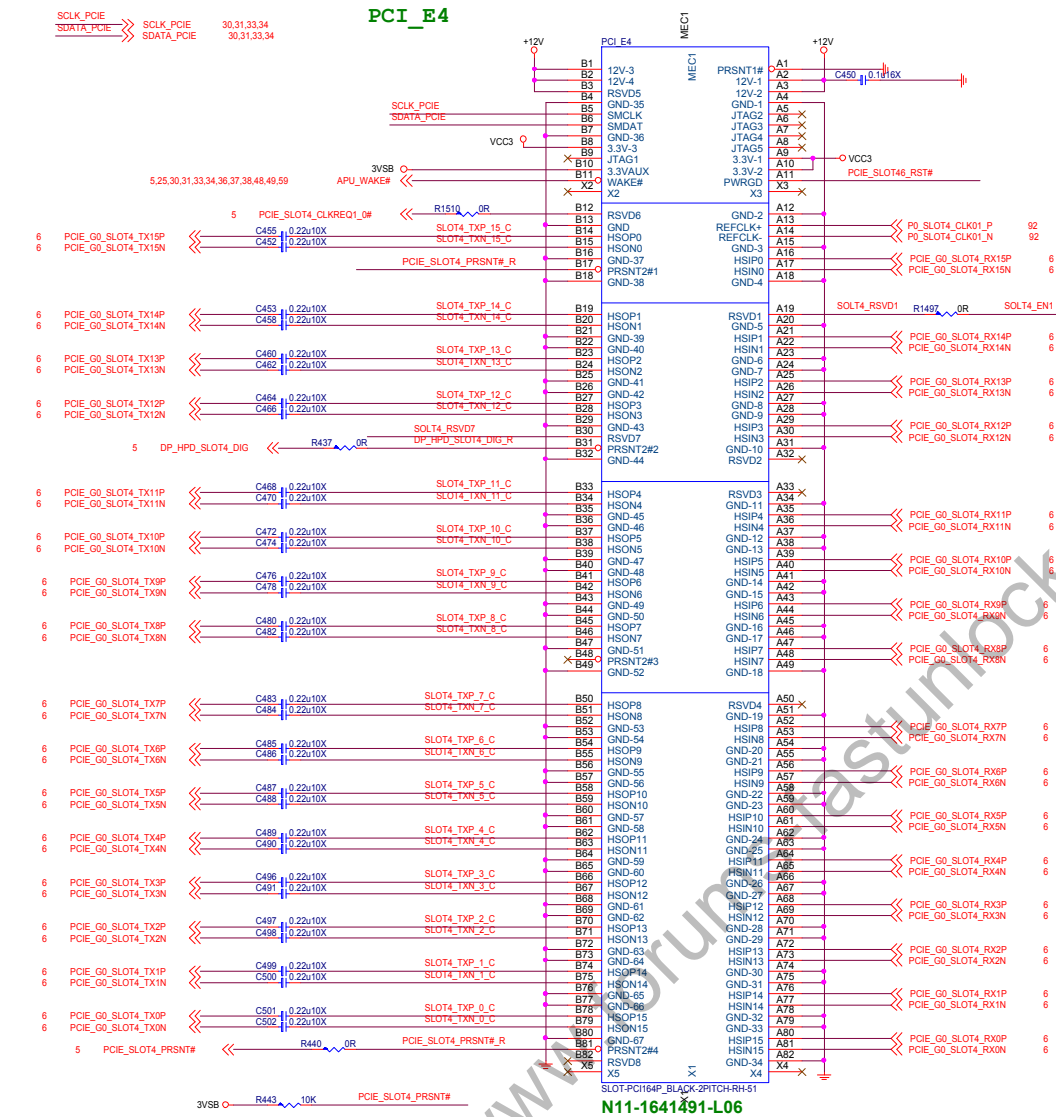
N93-04M0321-H06

PCI_E3

PCI EXPRESS X8 SLOT

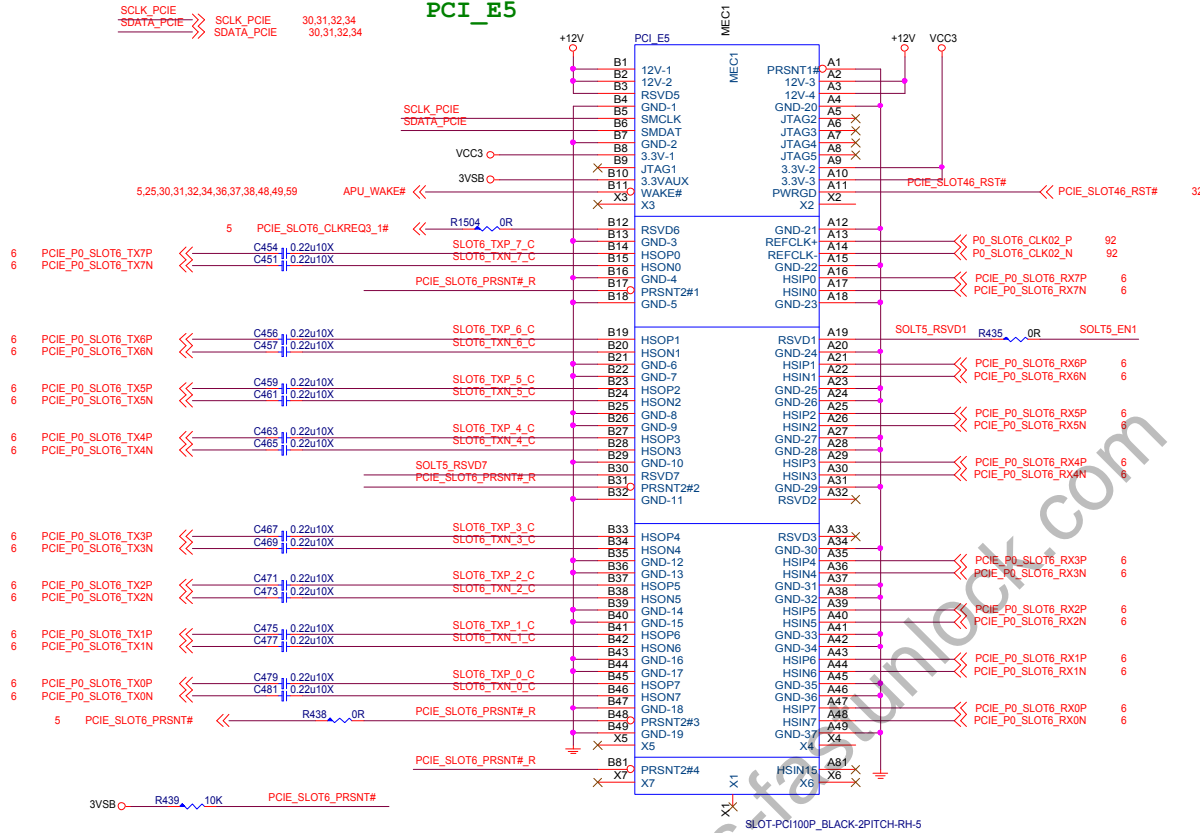


PCI EXPRESS X16 SLOT



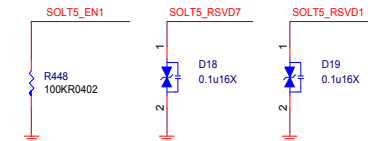
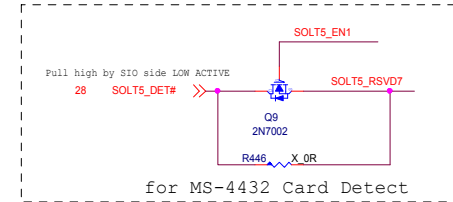
PCI EXPRESS X8 SLOT

PCI_E5



N11-1000221-L06

C71-56106J1-N07



PCI E2

The diagram illustrates the electrical connections for the PCI E2 connector. It shows a +12V supply at the top, a PCI E2 connector on the left, and a +12V supply on the right. The connector pins are labeled B1 through B18. The signals and their connections are as follows:

- B1: +12V
- B2: 12V
- B3: RSVD
- B4: GND
- B5: SMCLK
- B6: SMDATA
- B7: GND#B7
- B8: 3.3V
- B9: JTAG1
- B10: 3.3VAUX
- B11: WAKE_#
- B12: RSVD#B12
- B13: GND#B13
- B14: HSOP0+
- B15: HSOP0-
- B16: HSIOP0+
- B17: HSIOP0-
- B18: GND#B18

The signals on the right side of the diagram are:

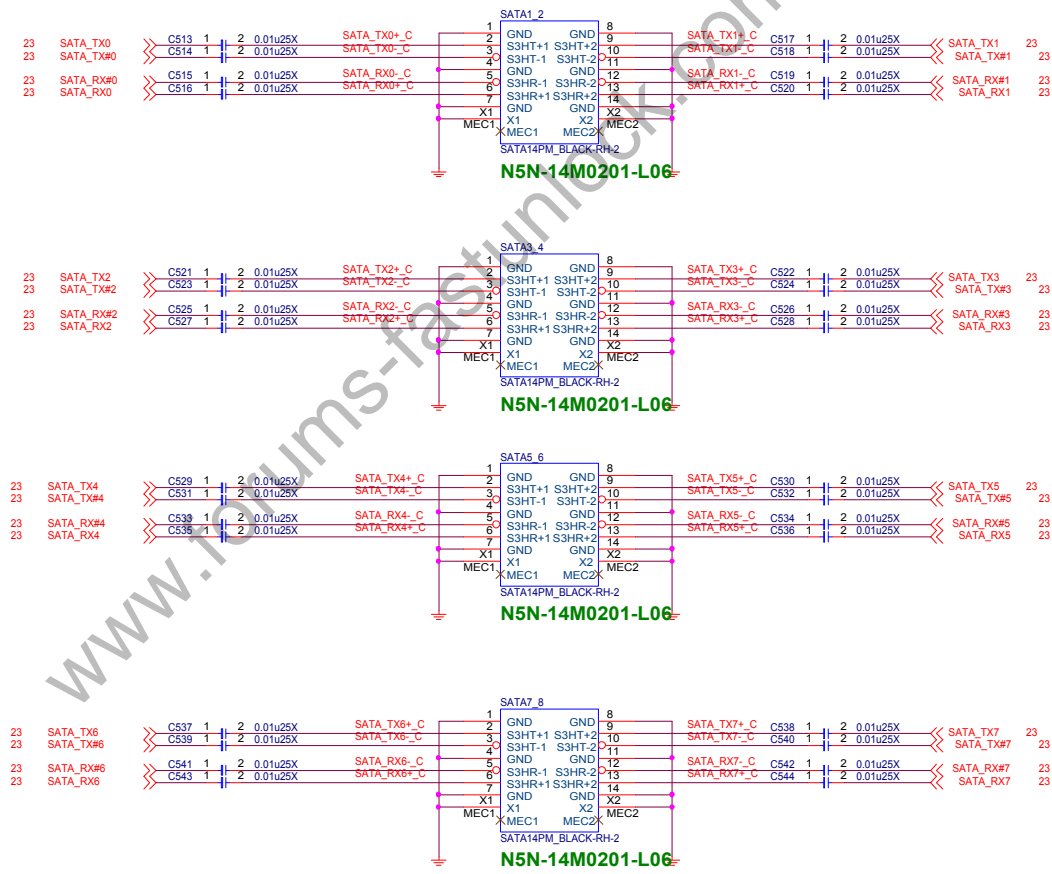
- A1: PRSNT1_#
- A2: 12V#A2
- A3: 12V#A3
- A4: GND#A4
- A5: JTAG2
- A6: JTAG3
- A7: JTAG4
- A8: JTAG5
- A9: 3.3V#A9
- A10: 3.3V#A10
- A11: PWRGD
- A12: X1
- A13: X12
- A14: REFCLK+
- A15: REFCLK-
- A16: GND#A15
- A17: HSIO0+
- A18: HSIO0-
- A19: GND#A18
- A20: X2

Connections are shown with lines and labels. Some connections are marked with 'X' and a red 'X' symbol, indicating a specific connection point or a warning.

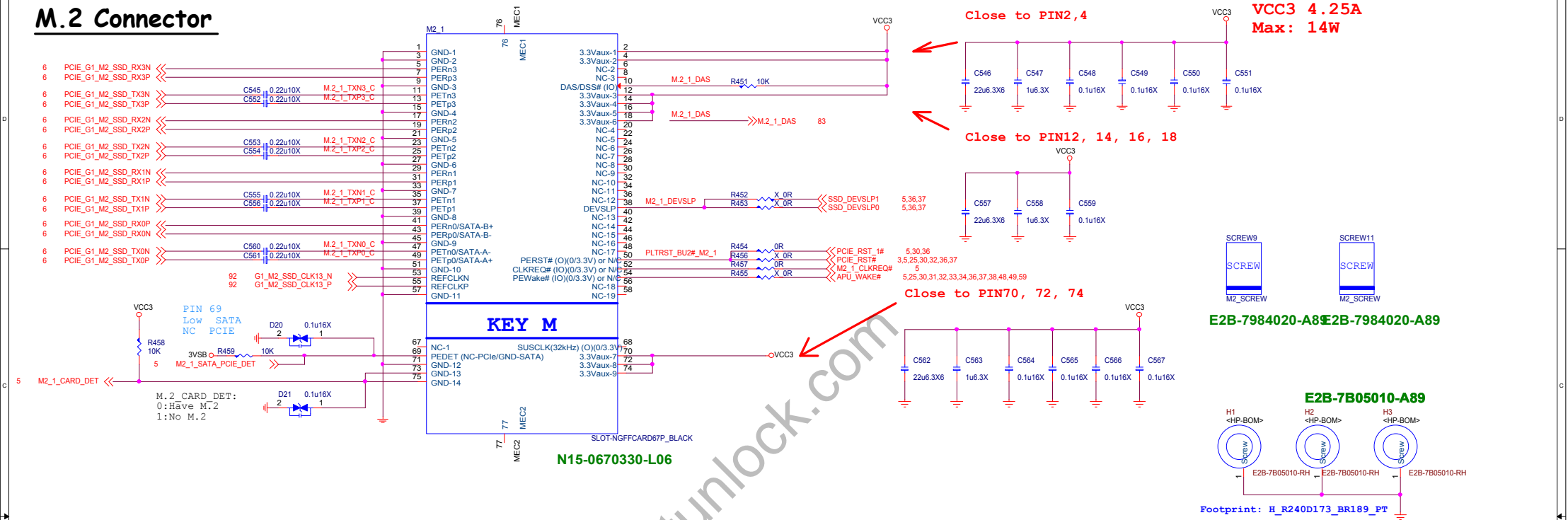
SCLK_PCIE		SCLK_PCIE	30,31,32,33
SDATA_PCIE		SDATA_PCIE	30,31,32,33

+3.3V - 6.0A

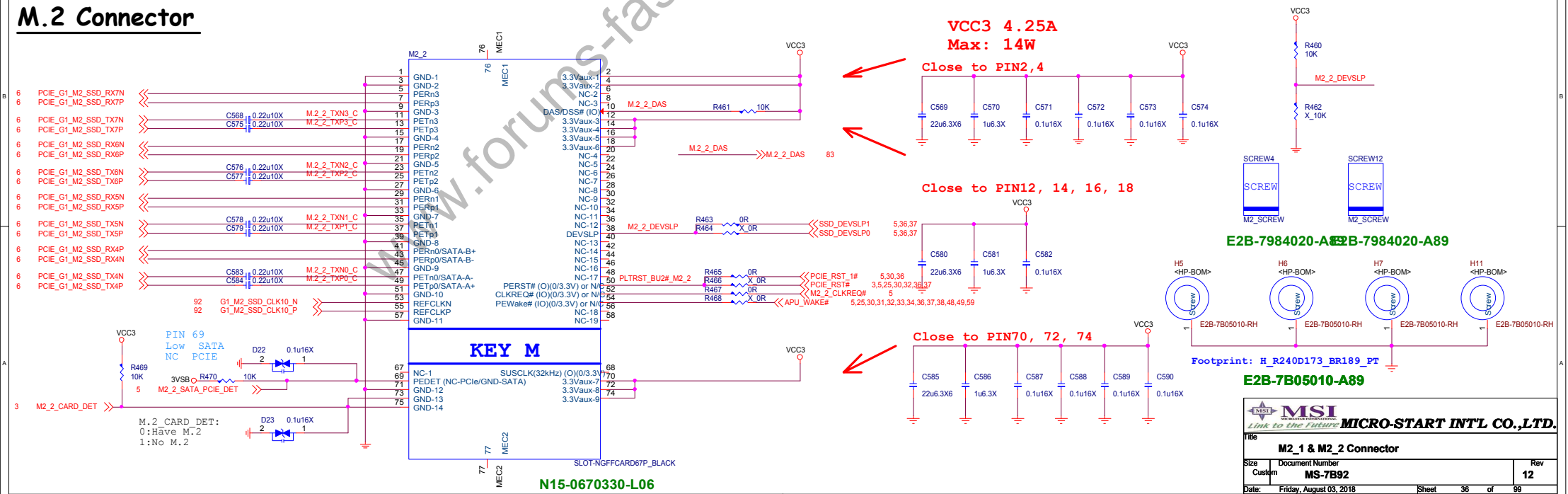
SATA Connector



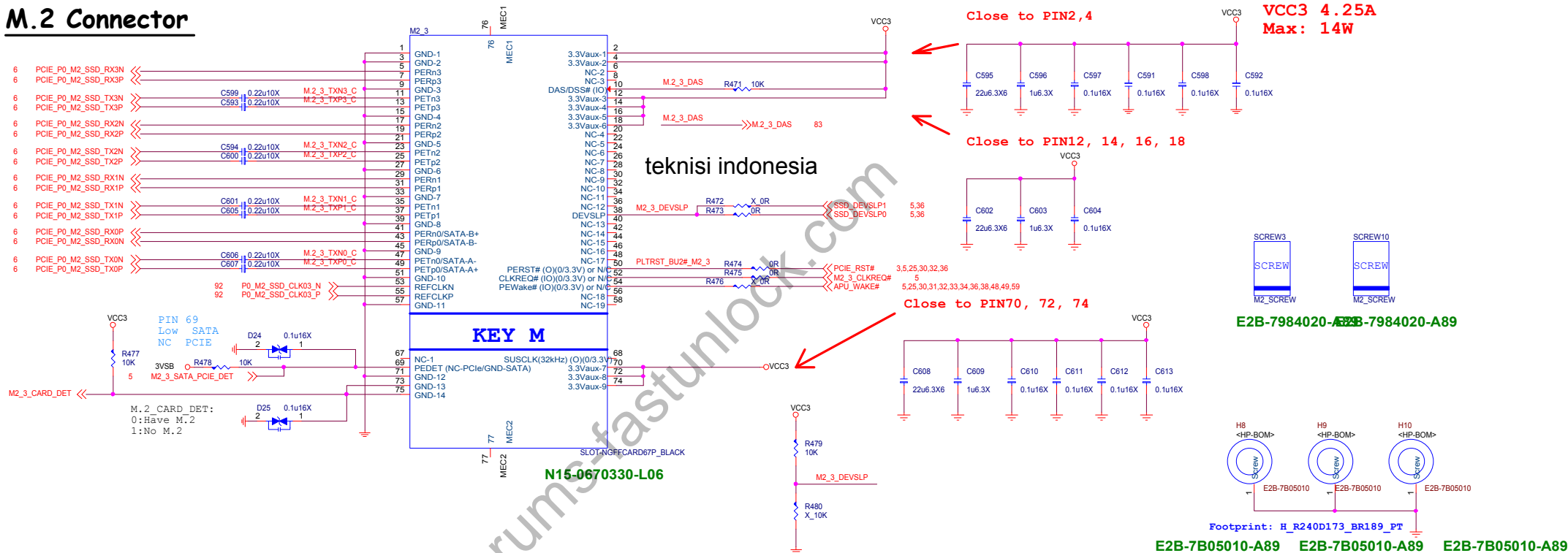
M.2 Connector

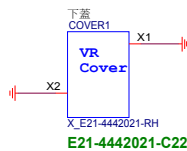
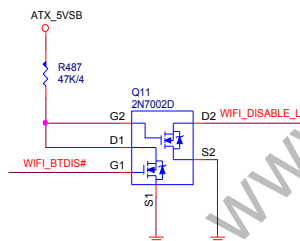
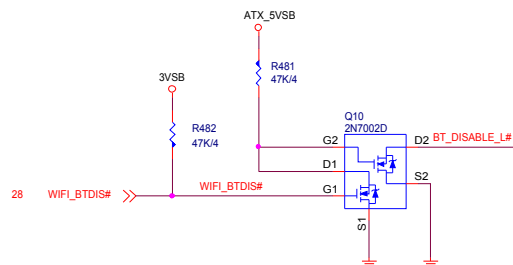
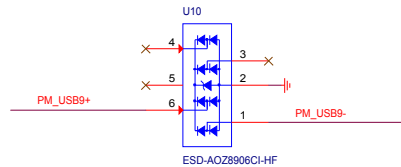
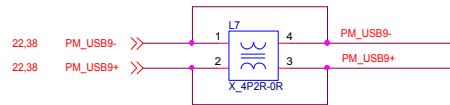


A.2 Connector



M.2 Connector



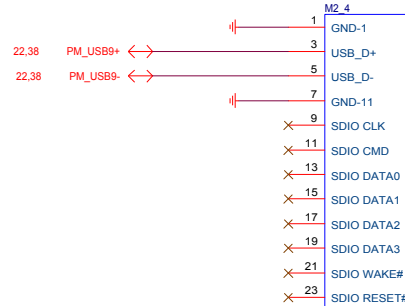


鍍WIFI1 Module螺絲 E43-1204046-P65 鍍WIFI1 Module螺絲 E43-1204046-P65

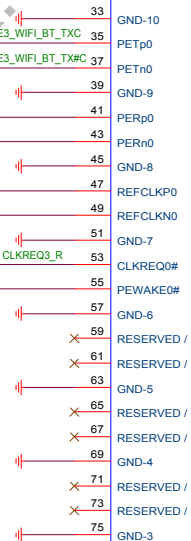
E43-1204046-P65

E43-1204046-P65

604-4442-040



KEY E



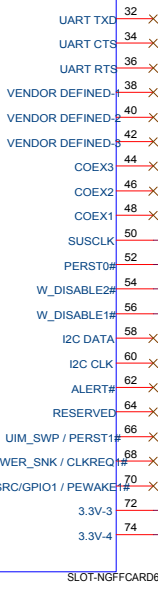
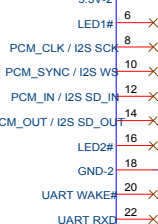
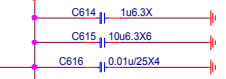
N15-0670610-L06



10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.
10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.

780mA

3VSB



MSI MICRO-START INTL CO.,LTD.

Title			M2_4 WIFI+BT		
Size			Document Number		
Date			MS-7B92		
Rev			12		
Date			Friday, August 03, 2018		
Sheet			38 of 99		

5,15,17,47,53,66,71,78,79,84,85,86,91,92
5,15,17,47,53,66,71,78,79,84,85,86,91,92

SPD_SMBUS_CLK
SPD_SMBUS_DATA

R494 0R SCLK_NCT5635_FAN
R488 0R SDA_NCT5635_FAN

40 CPUFAN1_FAULT
41 CPUFAN2_FAULT
40 CPUFAN1_FM
41 CPUFAN2_FM

21 VDD
19 SCL
20 SDA
22 INT#/LED/BEEP

GPIO00 1 CPUFAN1_MODE
GPIO01 2 CPUFAN2_MODE
GPIO02 3 SYSFAN1_MODE
GPIO03 4 SYSFAN2_MODE
GPIO04 5 SYSFAN3_MODE
GPIO05 6 SYSFAN4_MODE
GPIO06 7 SYSFAN5_MODE
GPIO07 8 7802_EXTFAN1_MODE
GPIO15 15 7802_EXTFAN2_MODE
GPIO16 16 CPUFAN1_LED_OFF_BLINK
GPIO17 17 CPUFAN2_LED_OFF_BLINK

5605_2_A2
5605_2_A1
5605_2_A0

R489 X 10K
R491 X 10K
R493 X 10K

CPUFAN1_LED_OFF_BLINK
CPUFAN2_LED_OFF_BLINK

R496 X 10K
R497 X 10K

40
41
42
43
44
45
46

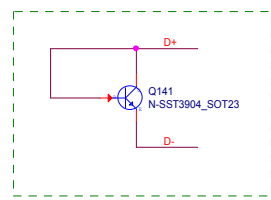
VCC3

R498 10K CPUFAN1_FAULT
R500 X 10K CPUFAN2_FAULT

use avoid S5 leakage

CPUFAN1_FM R499 1KR/4
CPUFAN2_FM R501 X 1KR/4

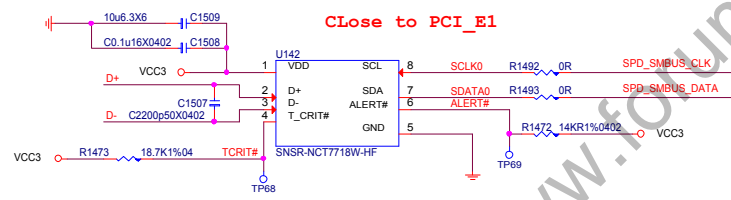
slave address :
Write 4CH
Read 4DH



Close to PCI_E4

NCT7718W

Close to PCI_E1



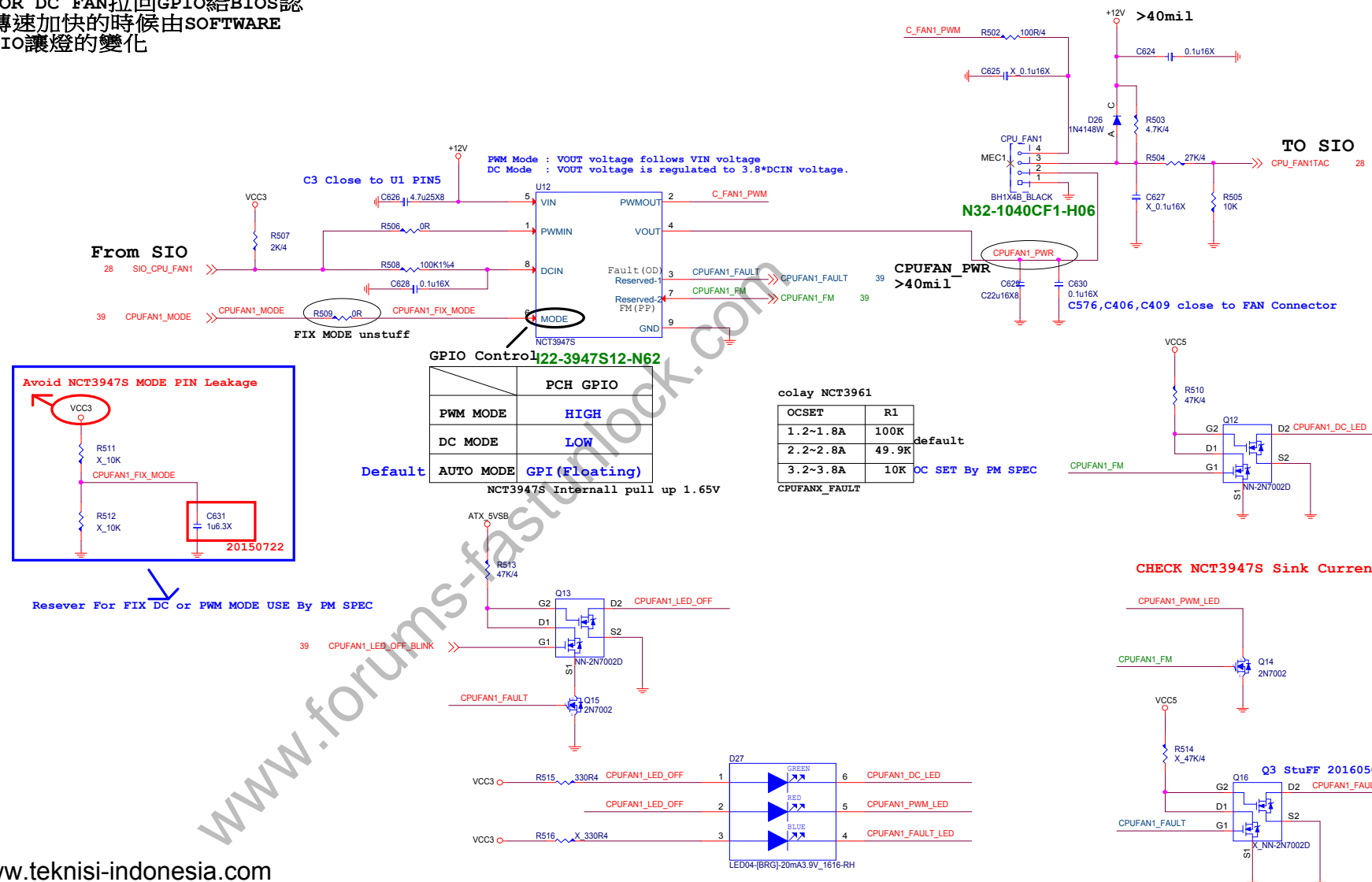
Layout notice:
1. Put the CI 2200pF to close the NCT7718W.
2. Add Ground Shielding For D+ and D- Traces.
3. D+/D- Route Has to be Away From the High Noise Area.
4. The Recommended Traces Width and Ground Shielding Spacing are 10mils.

NCT7718W SM Bus address is 98h (1001100xb) Default: ALERT# Output Comparator Mode

TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

1. PWM/DC/OC LED (現在是改成R/G/B3色LED)
2. GPIO可以由BIOS切換 PWM/DC MODE
3. OCP拉回GPIO給BIOS認
4. PWM OR DC FAN拉回GPIO給BIOS認
5. FAN轉速加快的時候由SOFTWARE控制GPIO讓燈的變化



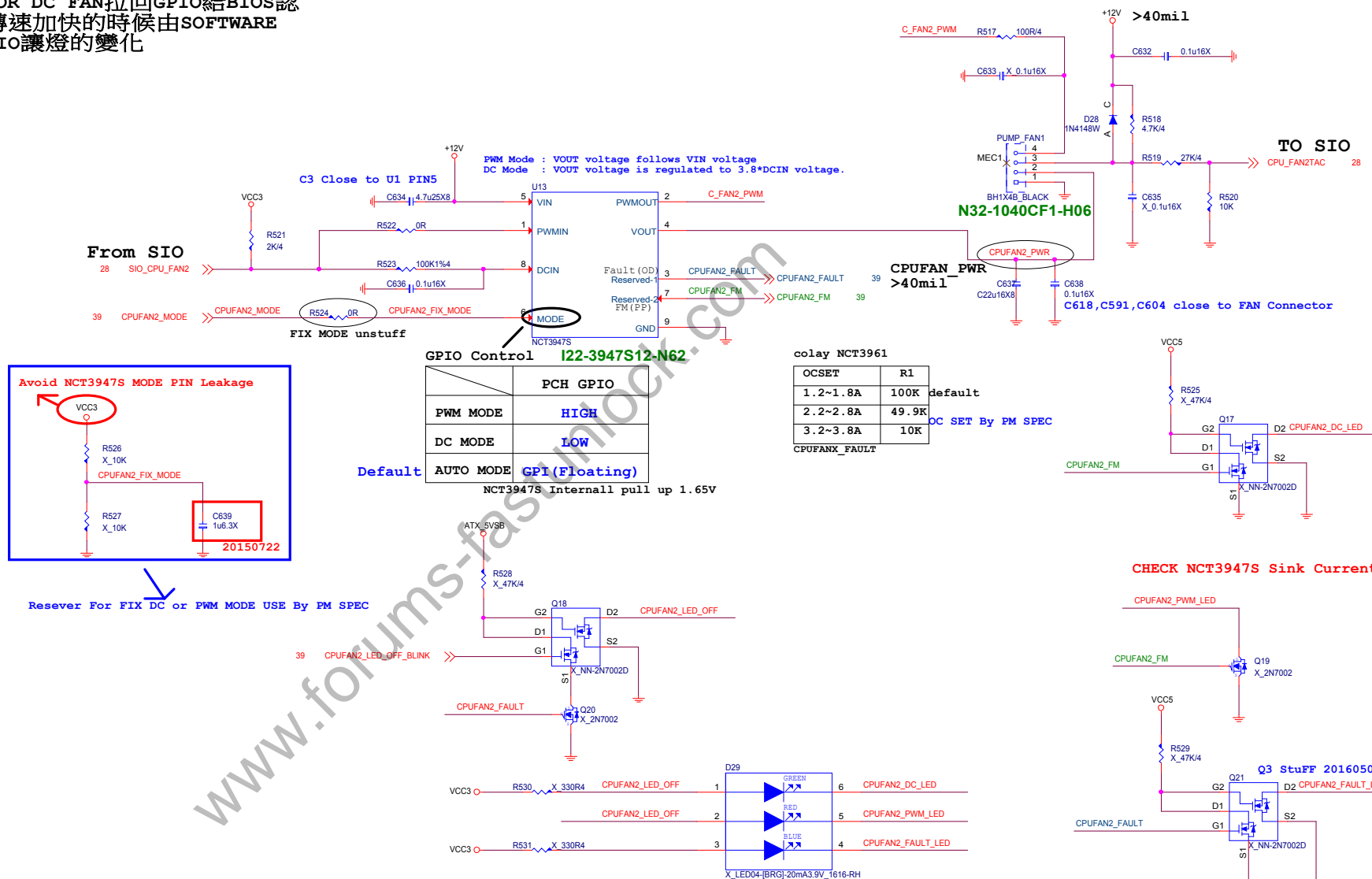
www.teknisi-indonesia.com

1. MODE : USE MODE PIN change FAN MODE (PWM or DC FAN)
2. FAULT : USE FAULT PIN Triger OVT/OCP Protection, LOW Atcive (Reserve NEW IC)
3. FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information (Reserve NEW IC)

TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

1. PWM/DC/OCF LED (現在是改成R/G/B3色LED)
2. GPIO可以由BIOS切换 PWM/DC MODE
3. OCP拉回GPIO給BIOS認
4. PWM OR DC FAN拉回GPIO給BIOS認
5. FAN轉速加快的時候由SOFTWARE控制GPIO讓燈的變化

PM SPEC更新成TYPE-K , 只改BOM



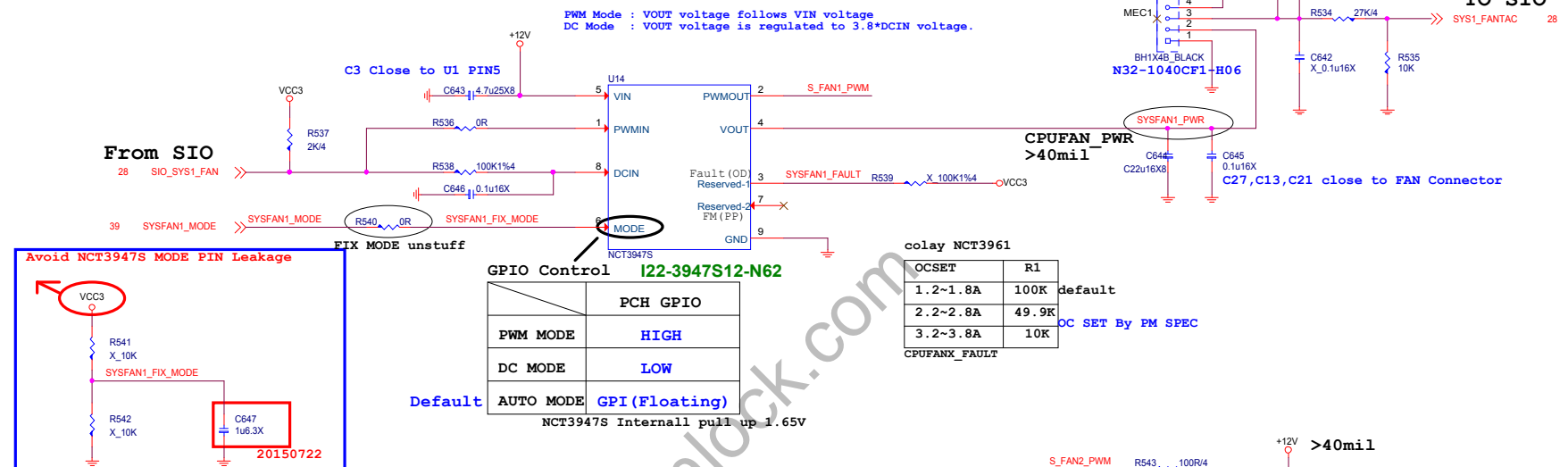
1. MODE : USE MODE PIN change FAN MODE (PWM or DC FAN)
2. FAULT : USE FAULT PIN Triger OVT/OCF Protection, LOW Atcive (Reserve NEW IC)
3. FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information (Reserve NEW IC)

CHECK NCT3947S Sink Current

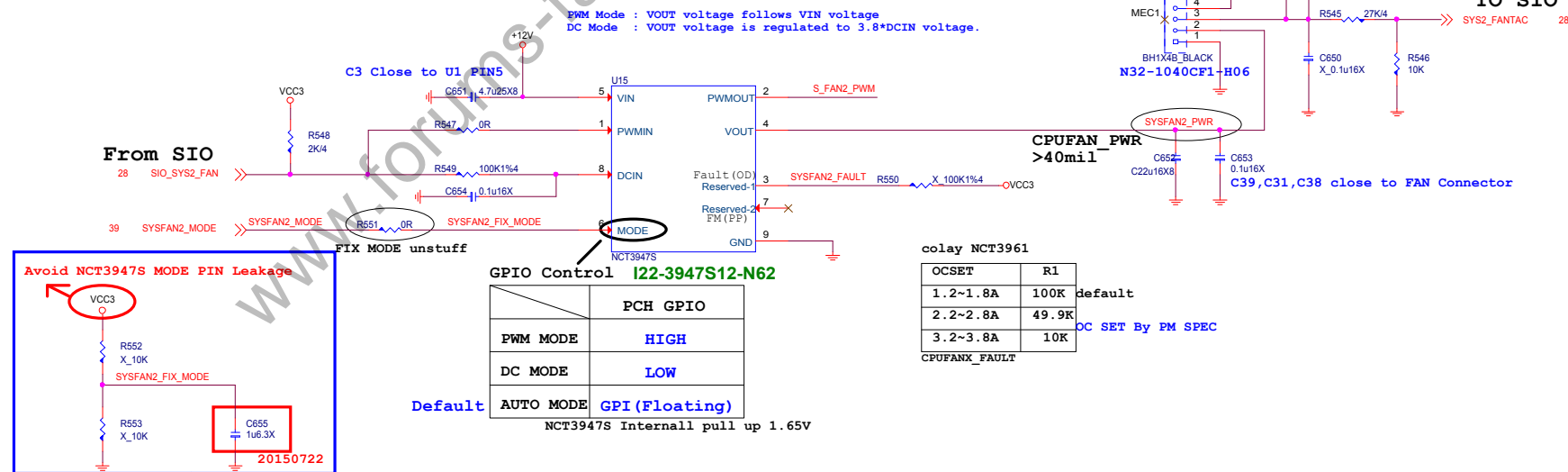
MSI LINK TO THE FUTURE MICRO-START INT'L CO., LTD.		
Title CPU FAN2-TYPE J(PUMP)		
Size Custom	Document Number MS-7B92	Rev 12
Date: Friday, August 03, 2018	Sheet 41	of 99

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1. Mode GPIO BIOS can switch PWM/DC Mode
2. FM:BIOS can read FAN PWM/DC Mode



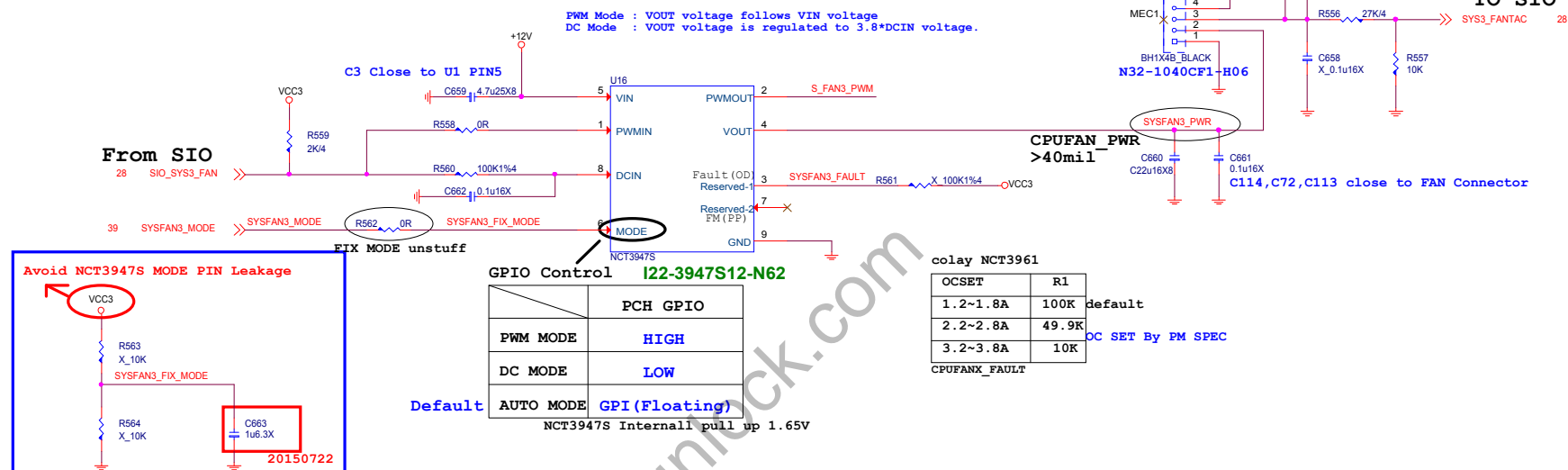
Resever For FIX DC or PWM MODE USE By PM SPEC



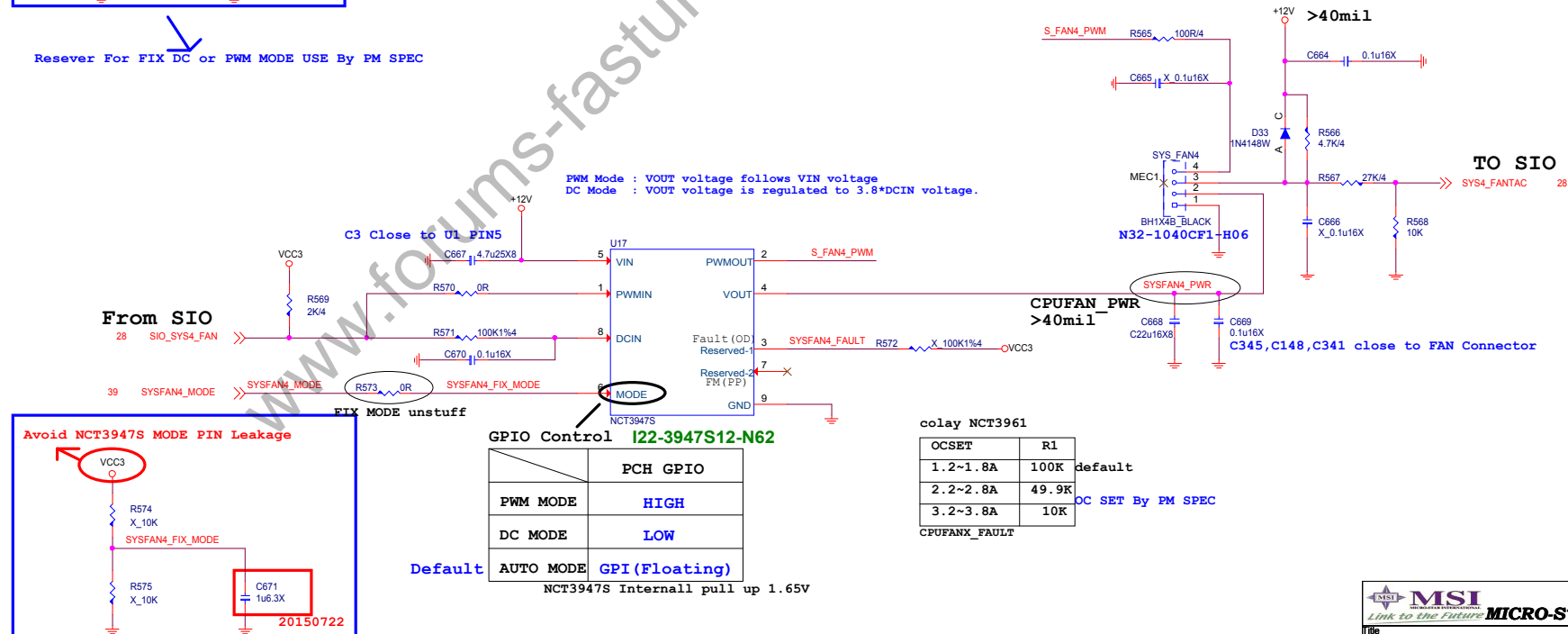
Resever For FIX DC or PWM MODE USE By PM SPEC

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1. Mode GPIO BIOS can switch PWM/DC Mode



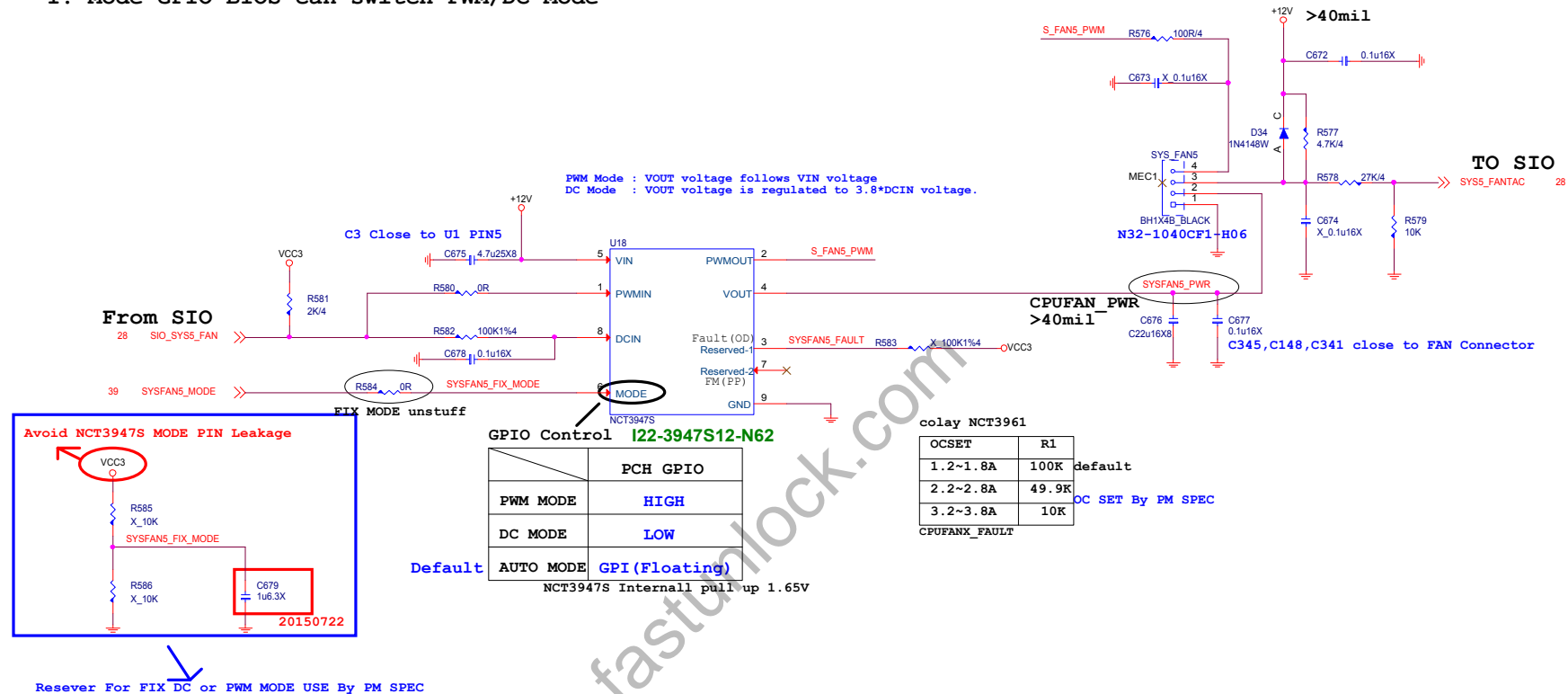
Reserver For FIX DC or PWM MODE USE By PM SPEC



Reserver For FIX DC or PWM MODE USE By PM SPEC

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1. Mode GPIO BIOS can switch PWM/DC Mode



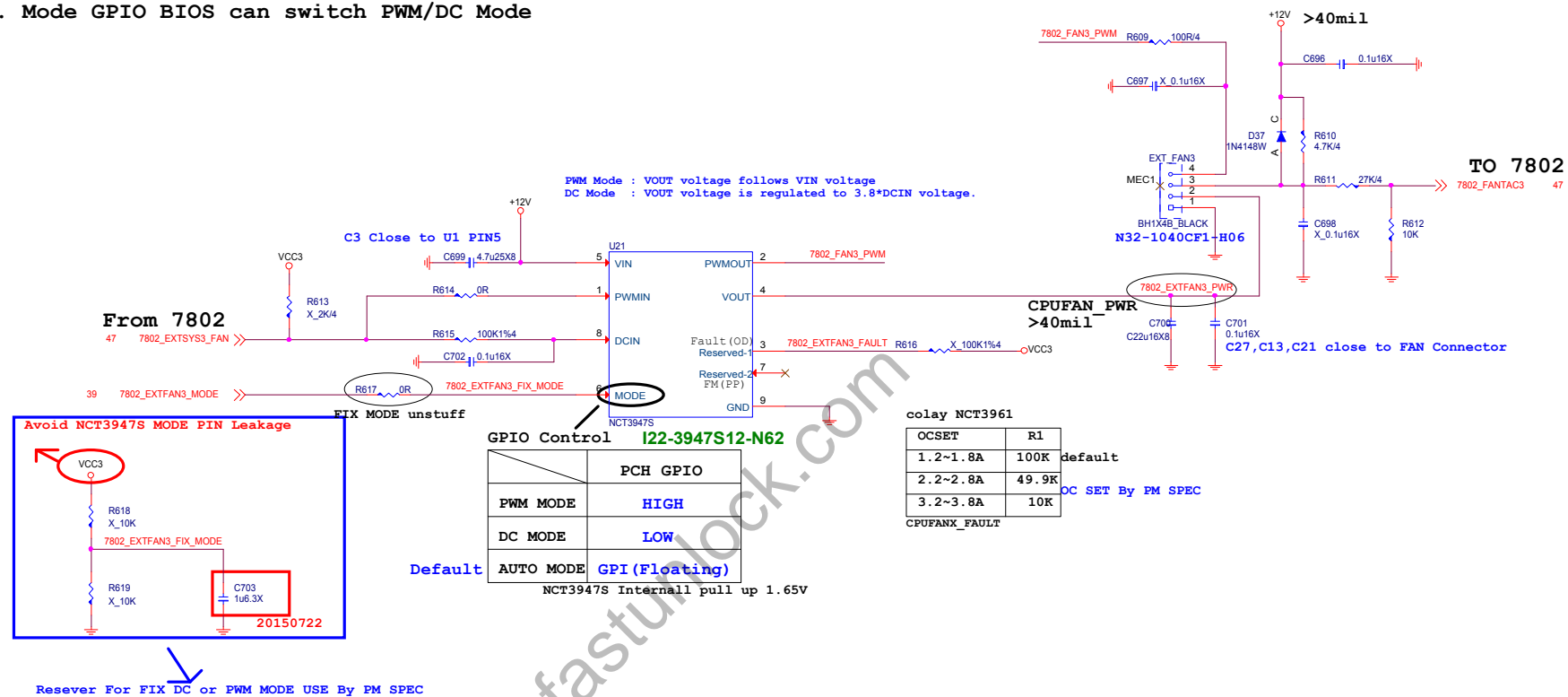
1. Mode GPIO BIOS can switch PWM/DC Mode

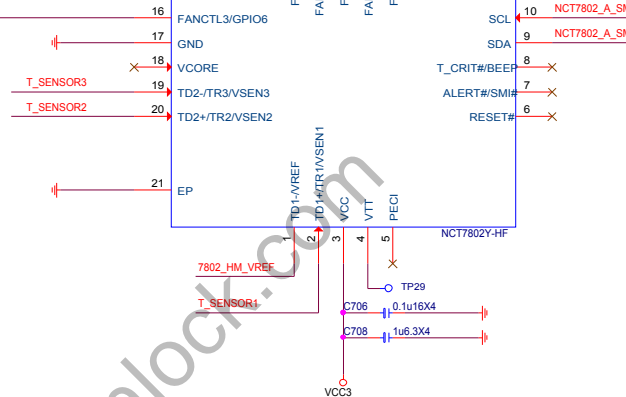
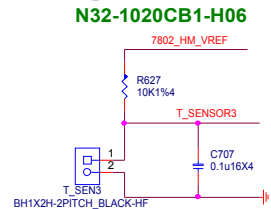


OCSET	R1
1.2~1.8A	100K
2.2~2.8A	49.9K
3.2~3.8A	10K

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

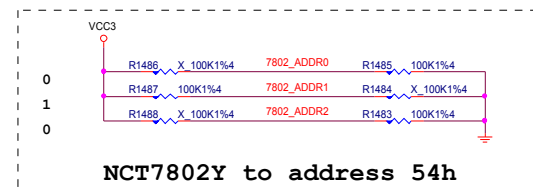
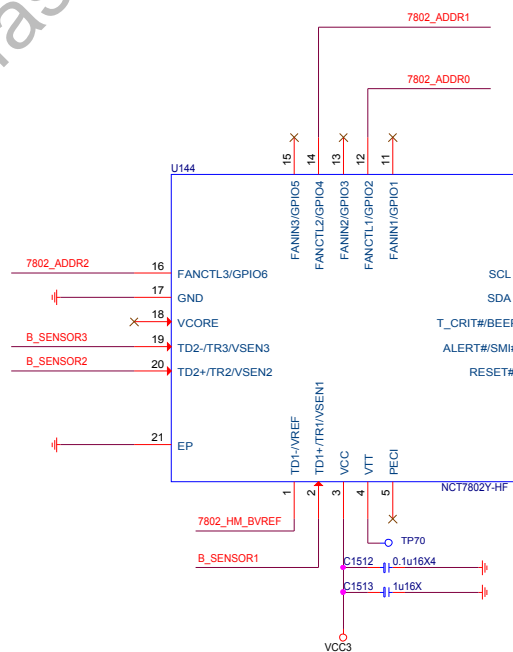
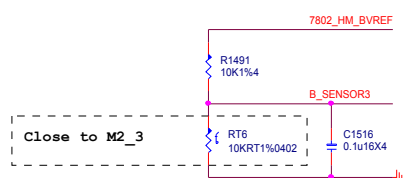
1. Mode GPIO BIOS can switch PWM/DC Mode



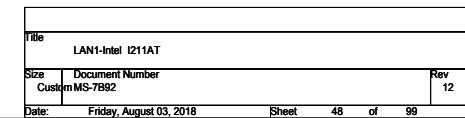
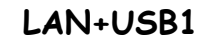


NCT7802Y to address 50h

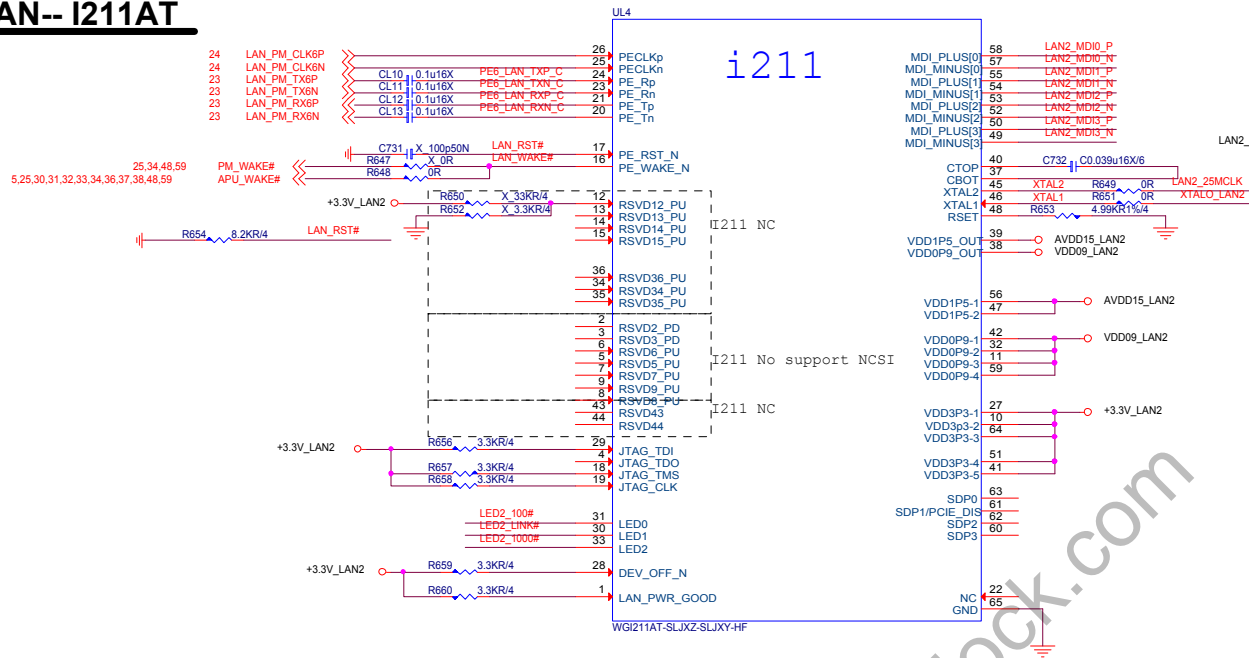
```
Sense T_SEN1 control EXTFAN1
Sense T_SEN2 control EXTFAN2
Sense T_SEN3 control EXTFAN3
```



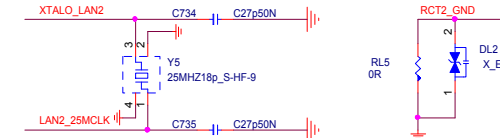
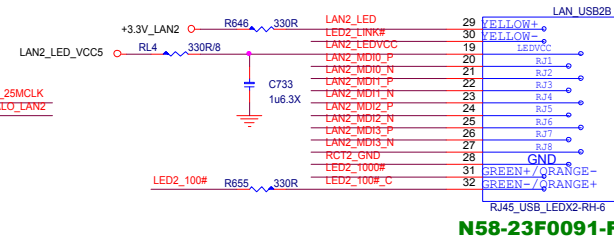
LAN Connector



LAN-- I211AT

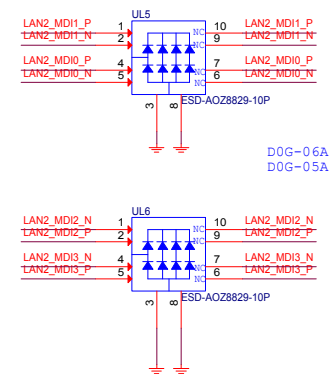
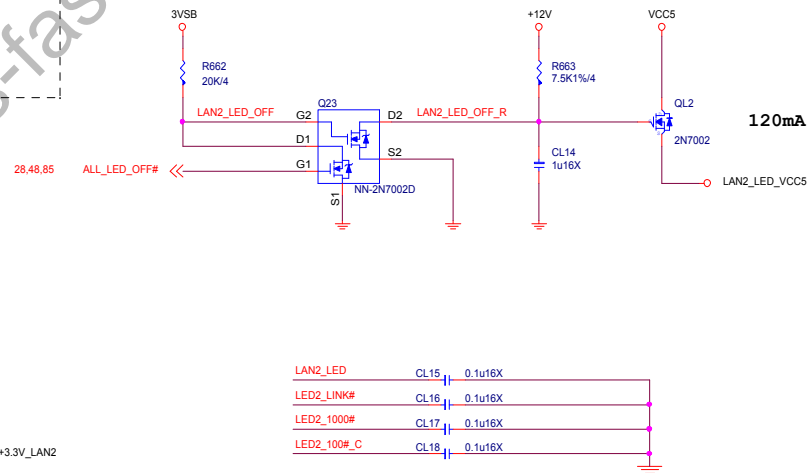
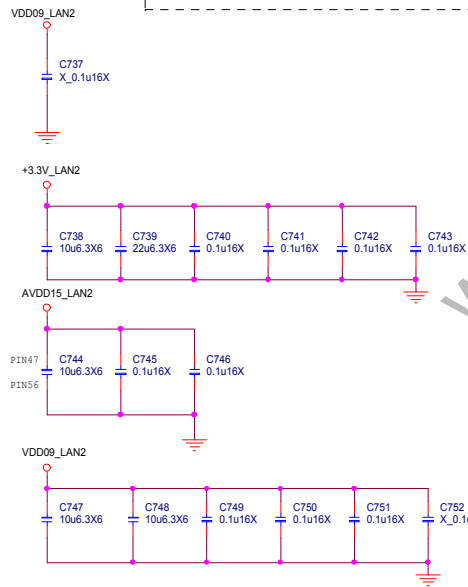
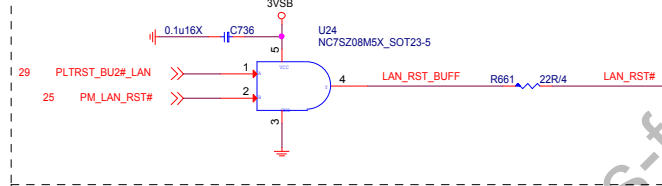


LAN+USB2



2016.07.21 Add

Disable LAN Function



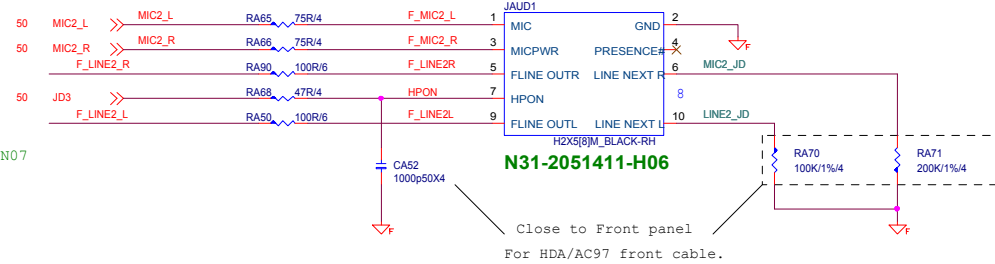
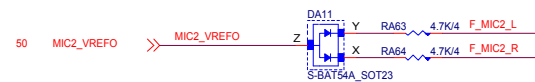
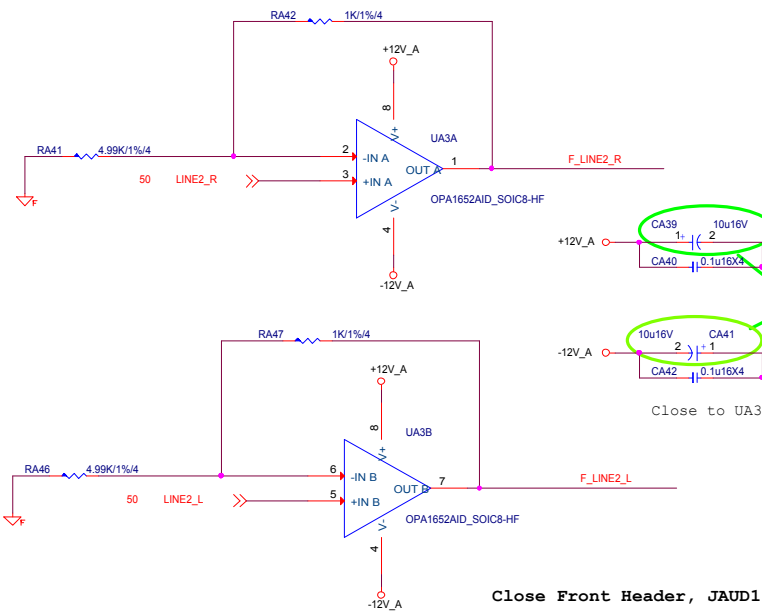
D0G-06A050C-A68
D0G-05A0300-I14

Ess9023

Removed Ess9023

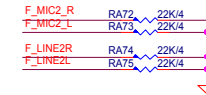
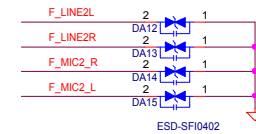
Analong SW1

Analong SW2

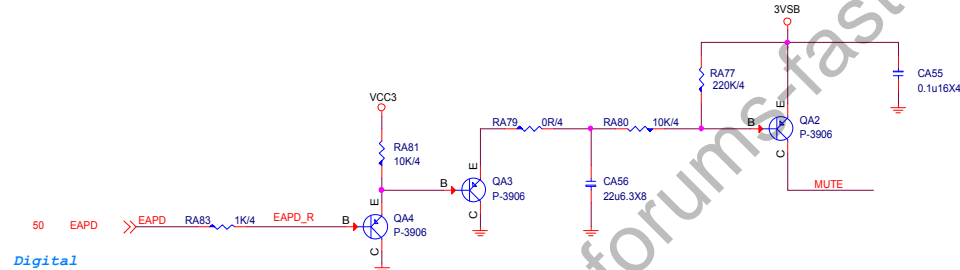


Close to Jack

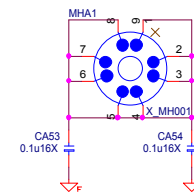
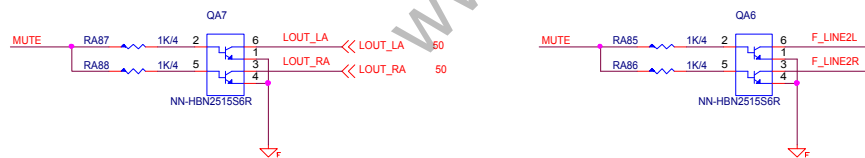
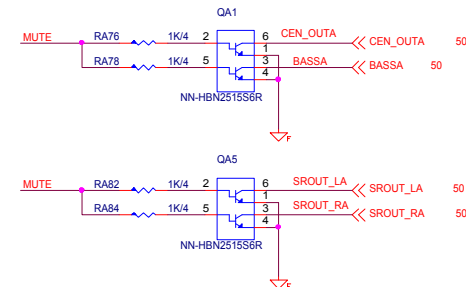
ESD protect
D0G-2950500-S10
D0G-3010510-I05



Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out)

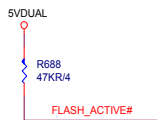
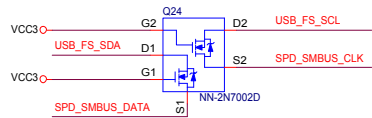
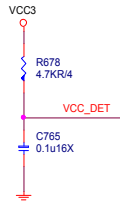
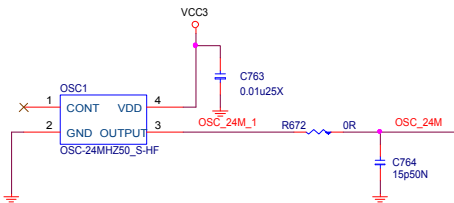


(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6, CA7, CA12, CA13, CA23, CA24 to TVS)



USB Flash BIOS

Host USB connector



Reserved for when F75501 Hotkey device fail use

* All close to Front IO side

5,15,17,39,47,66,71,78,79,84,85,86,91,92
5,15,17,39,47,66,71,78,79,84,85,86,91,92

SPD_SMBUS_DATA
SPD_SMBUS_CLK

5,28,54,65,77,78,79,95

5,28,54,65,74,75,80,81,92

SLP_S5#

SLP_S3#

84 FLASH_ACTIVE#

VCC_DET

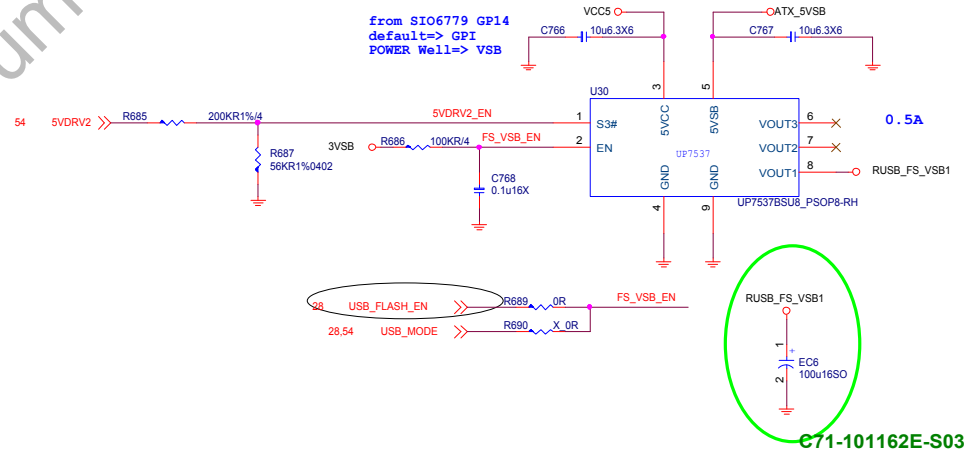
CLK_STRAP

Pin 24

Floating PIN14=24Mhz input

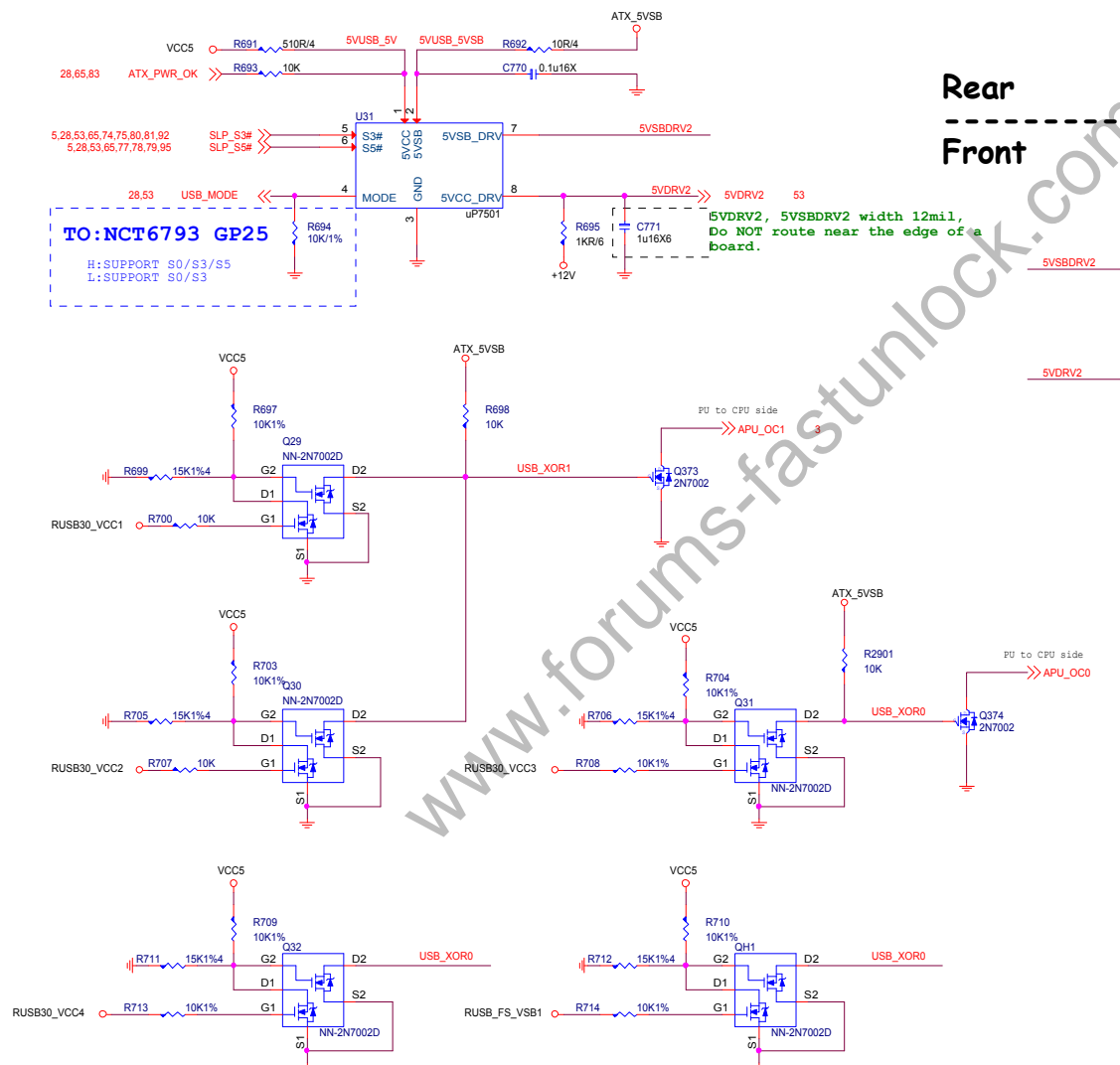
Pull-down Pin14=48Mhz input

REAR Flash BIOS USB PORT

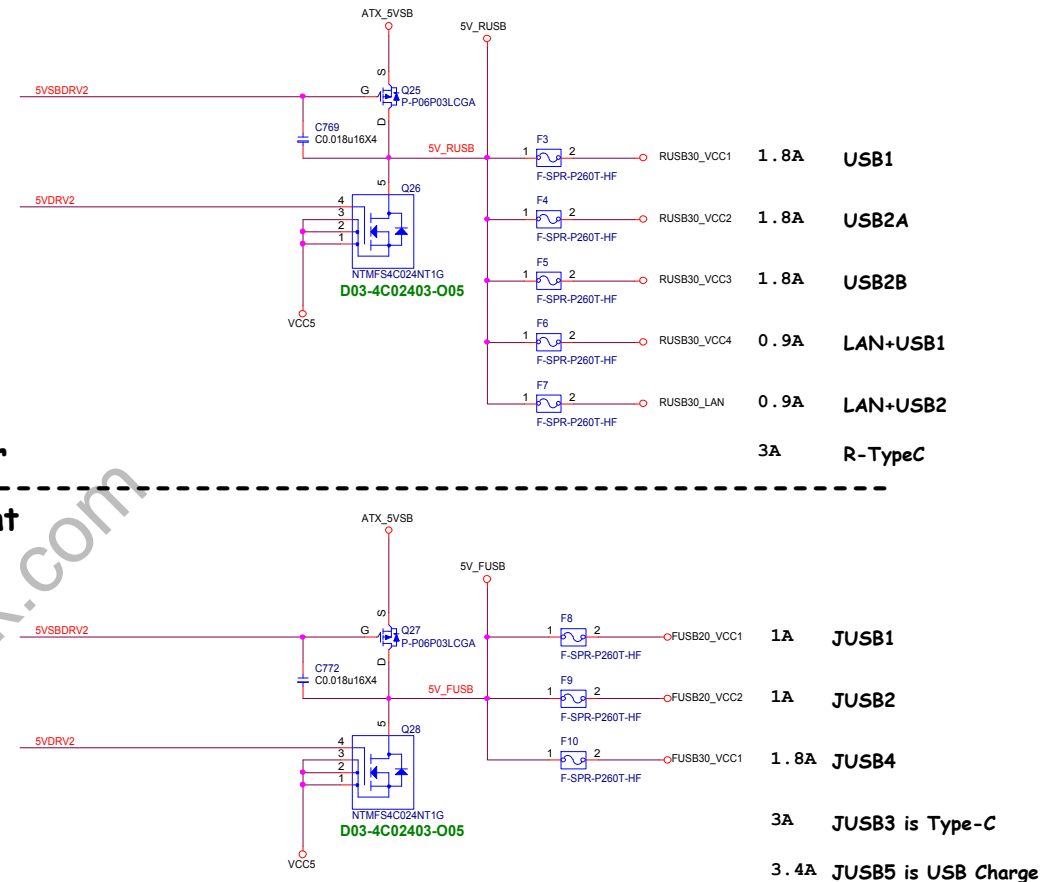


C71-101162E-S03

USB Power

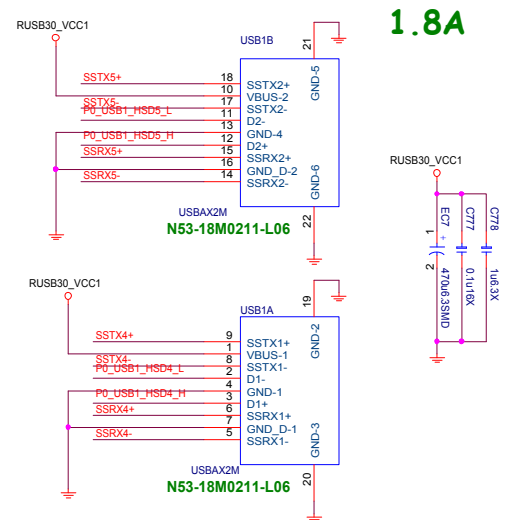
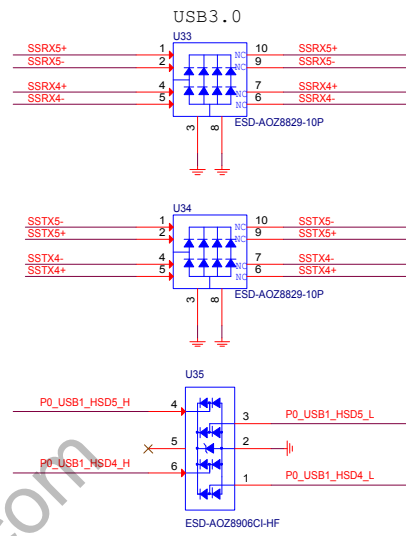
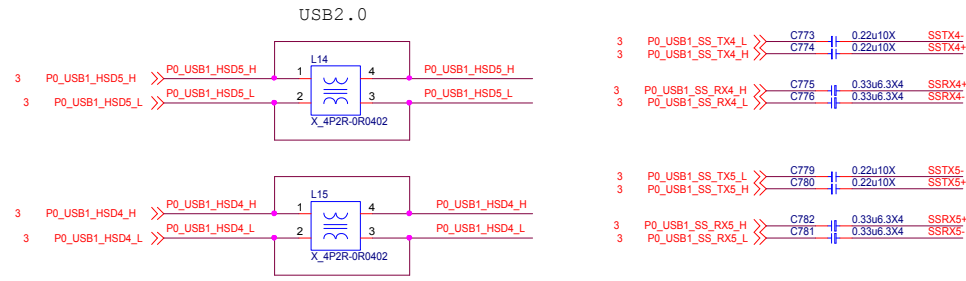


Rear
Front

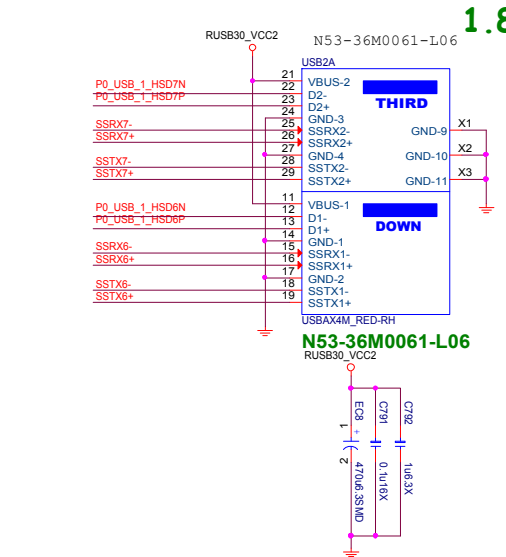
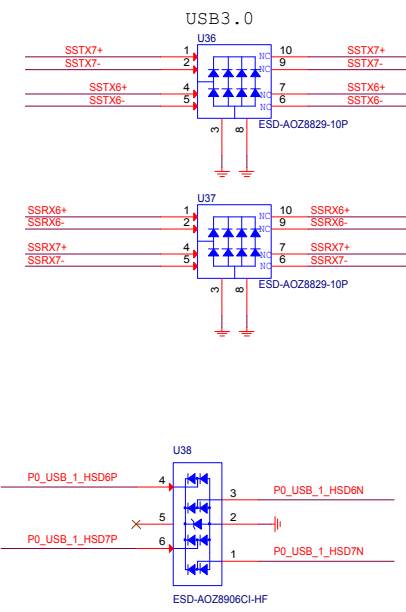
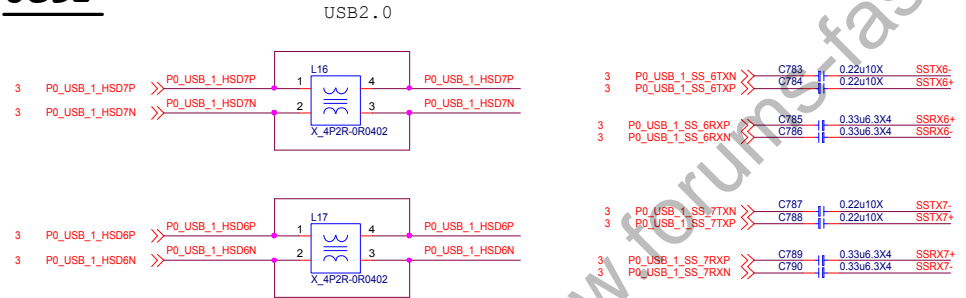


	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

USB1

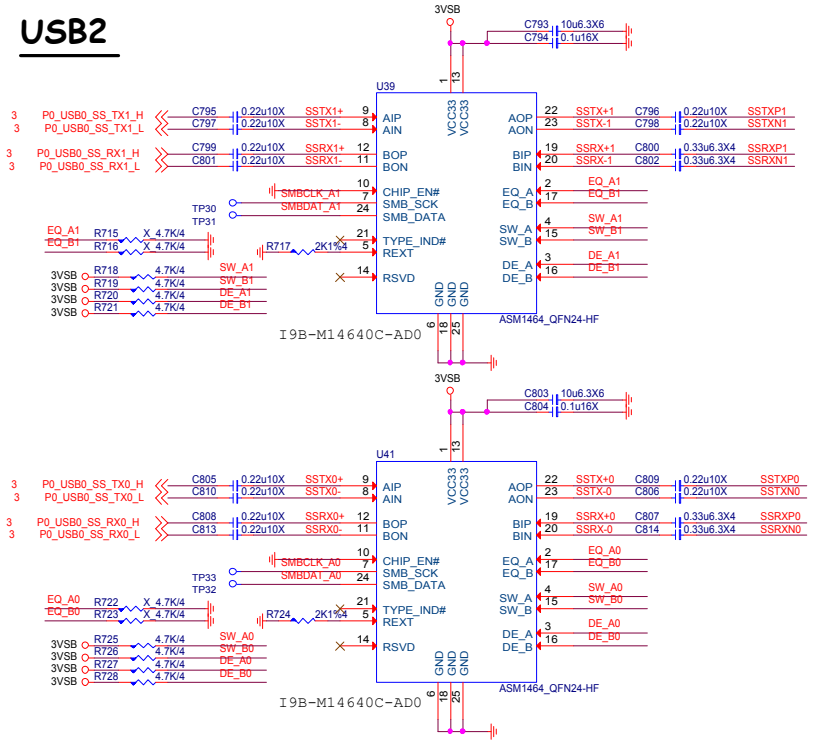


USB2

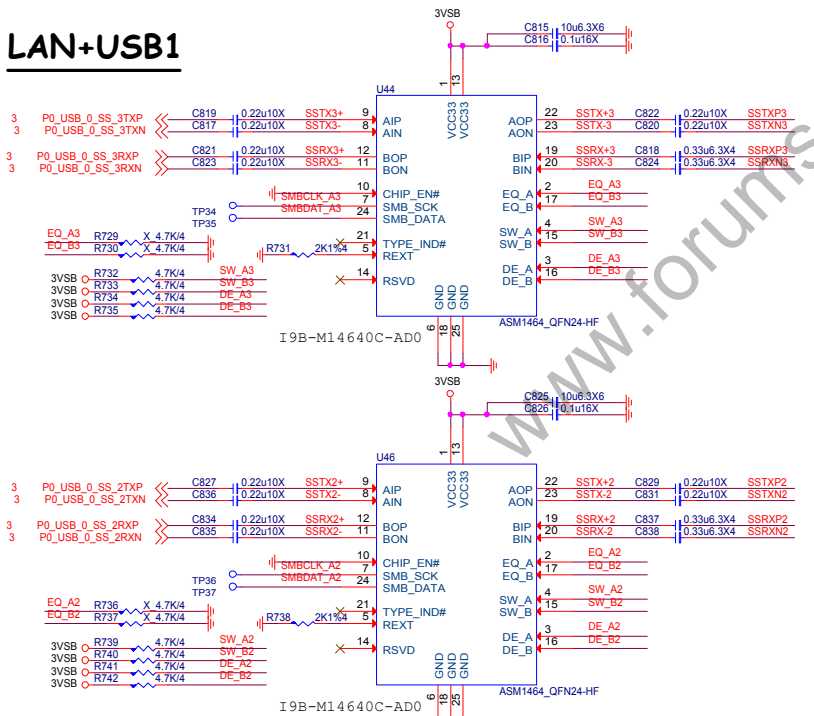


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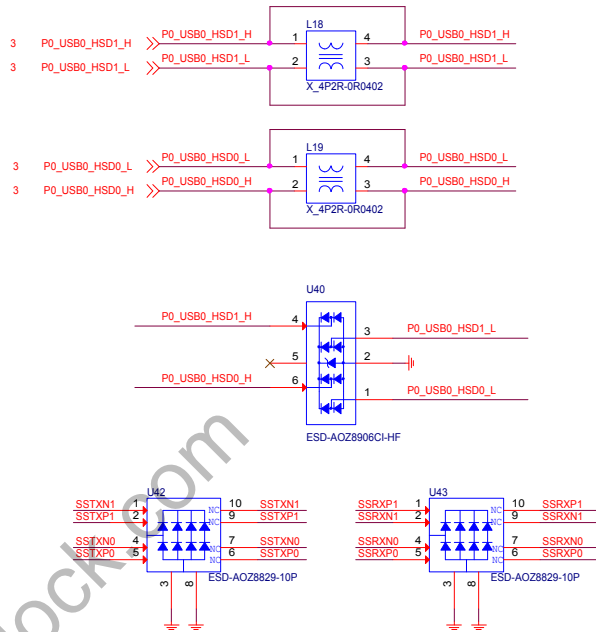
USB2



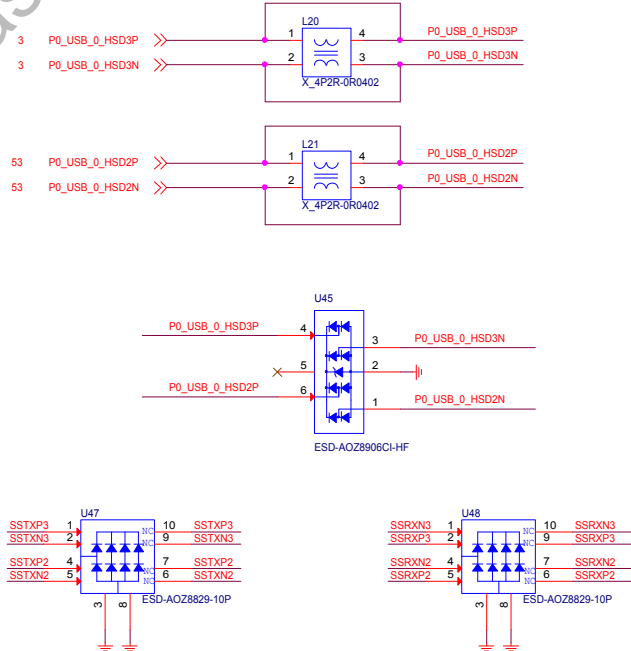
LAN+USB1



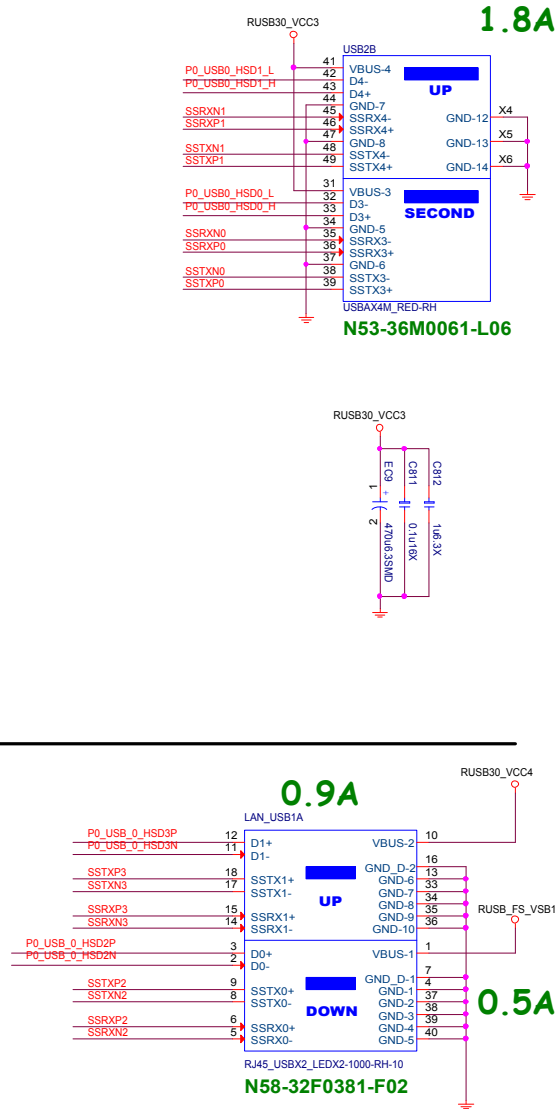
USB2.0



USB2.0

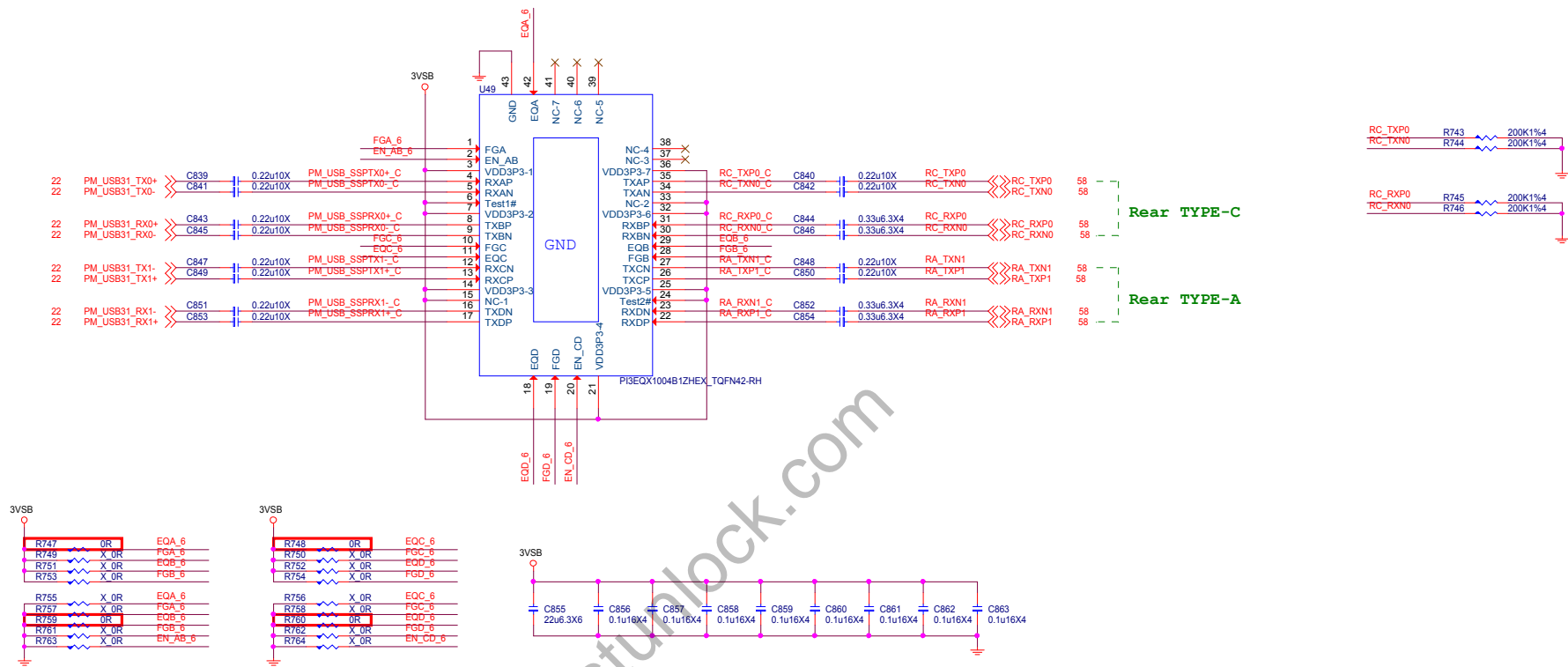


1.8A



0.9A

0.5A



EQ	dB	
0	12.4	0 to GND
R	8	68K to GND
F	10.6	NC
1	14.6	0 to VDD

FG	dB	
0	-1.6	0 to GND
R	-0.5	68K to GND
F	1.0	NC
1	2.7	0 to VDD

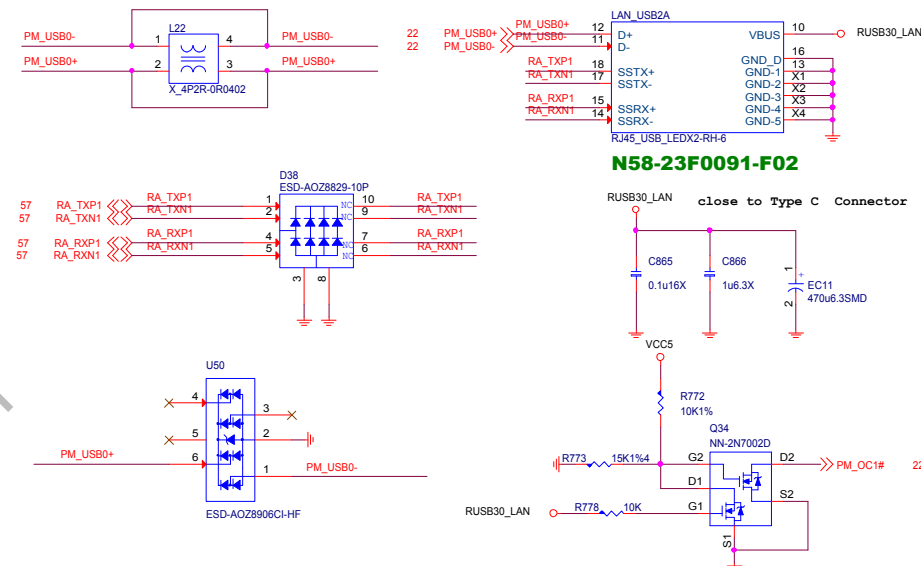
VBUS EN

Current Mode

USB Type-C MUX with Configuration Channel (CC)

IVCC : 356 μ A

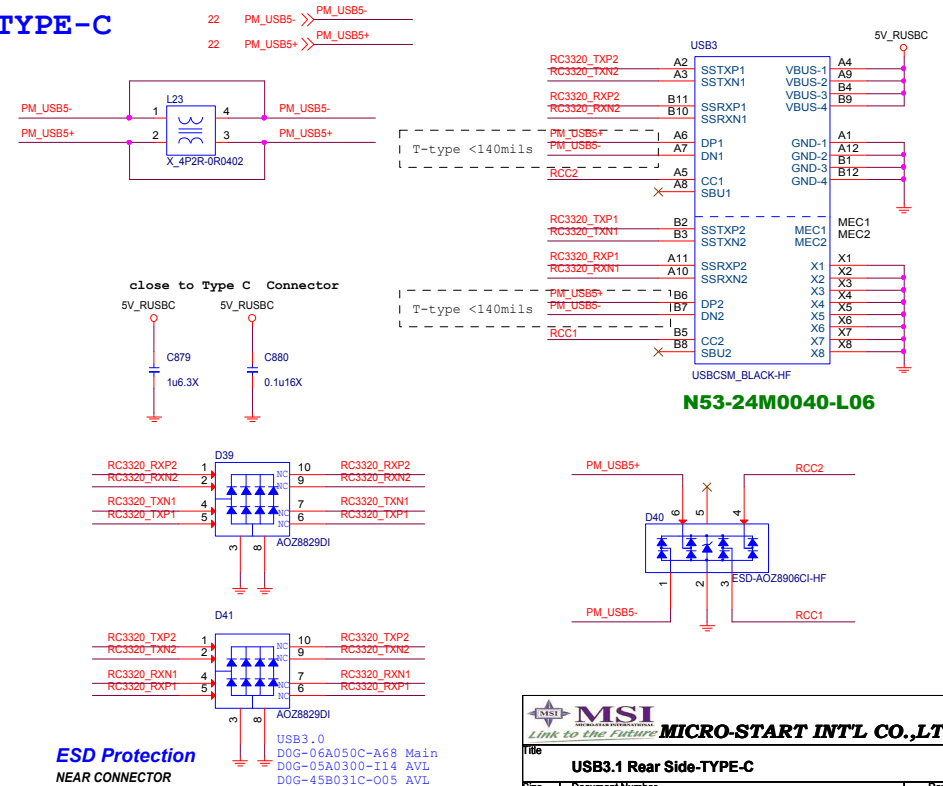
TYPE-A



LAN+USB2

N58-23F0091-F02

TYPE-C



ESD Protection
NEAR CONNECTOR

USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-O05 AVL

Use pure PCIE must provide CLK

Minimum gap should be greater of
>15mil with other signal.

Chip to Connector

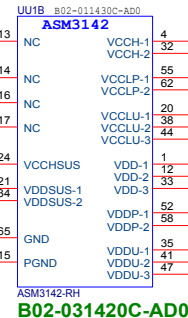
Front side USB3.1 TYPE C

Layout Guide:

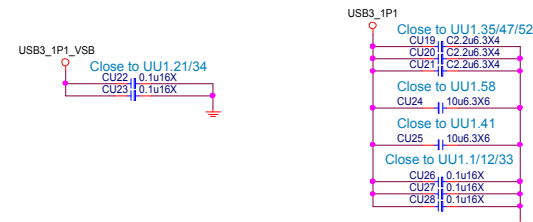
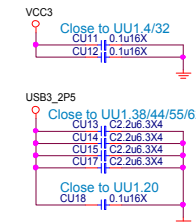
- 1.) USB3.1 to Connector Total Length < 1.5"
- 2.) VIA hole < 2

Power Consumption

	3.3V	3.3VSUS	2.5V	1.1V	1.1VSUS	Unit
ASM3142	TBD	TBD	TBD	TBD	TBD	mA
ASM2142	4	9	220	470	10	mA

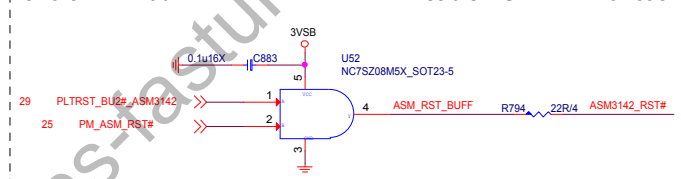


B02-031420C-AD0

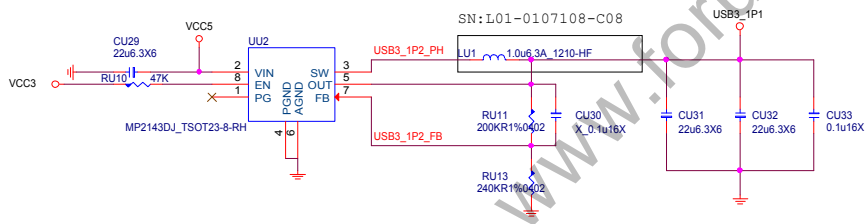


2016.07.21 Add

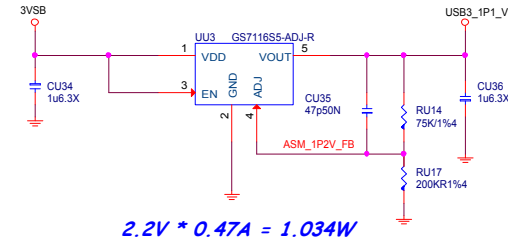
Disable ASM1142 Function



ASM3142 1.1v Core Power

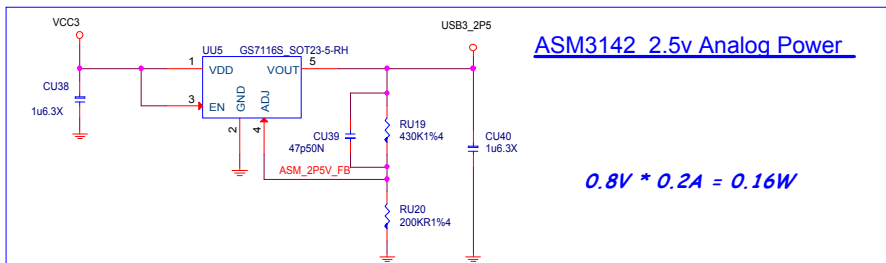


ASM3142 1.1v Suspend Power



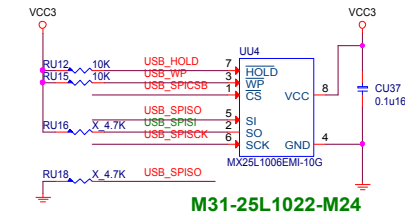
$$2.2V * 0.47A = 1.034W$$

ASM3142 2.5v Analog Power



$$0.8V * 0.2A = 0.16W$$

EEPROM



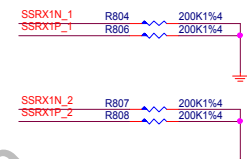
M31-25L1022-M24

M: M31-25L1022-M24 (1M)
S: M31-25X2023-W03 (2M)

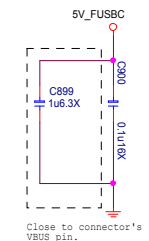
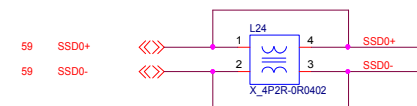
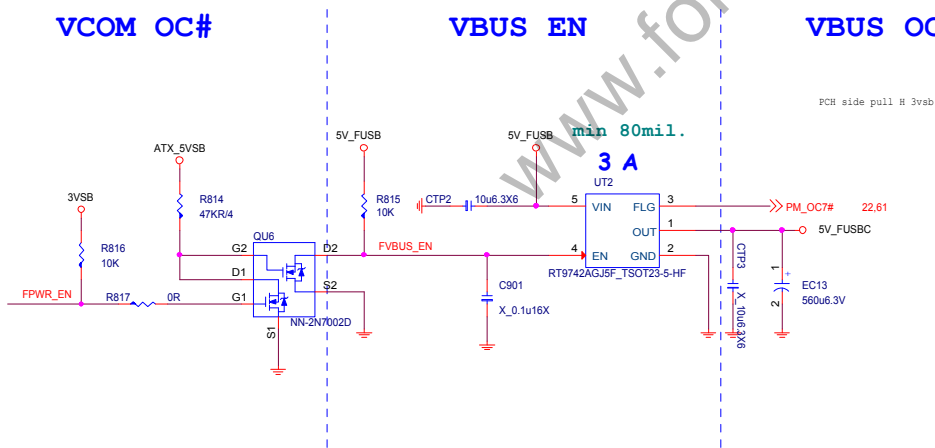
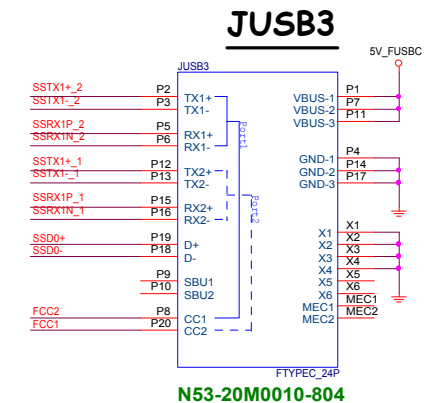
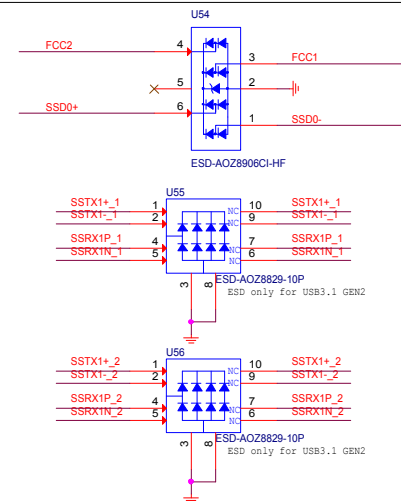
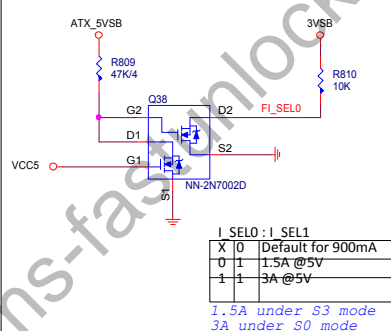
MSI MICRO-START INTL CO.,LTD.

Title			Rev		
ASM3142-1			12		
Size	Document Number			Date	
Custom	MS-7B92			Friday, August 03, 2018	
		Sheet	59	of	99

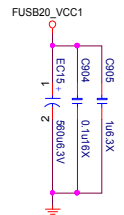
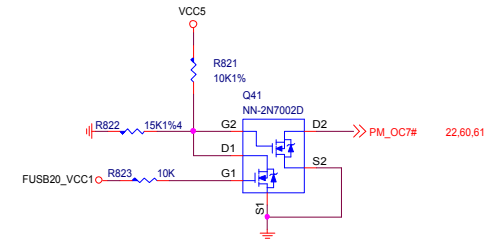
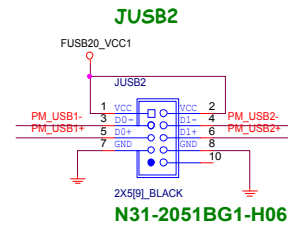
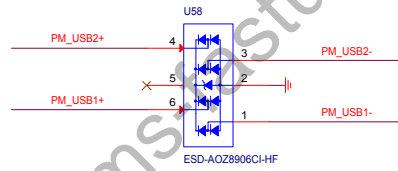
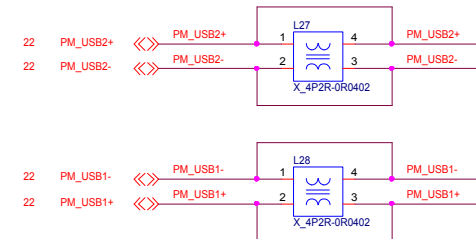
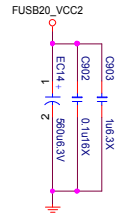
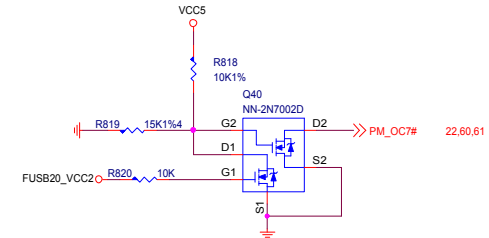
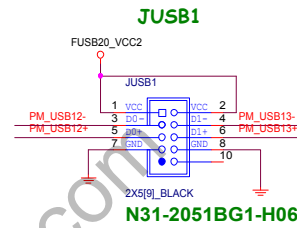
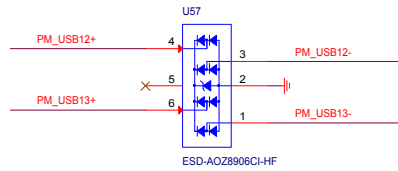
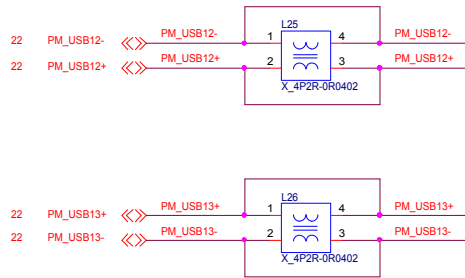
USB Type-C MUX with Configuration Channel (CC)



Current Mode

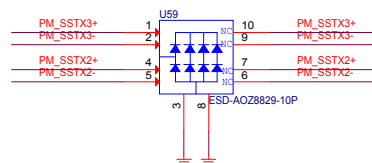
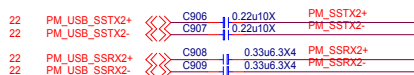


JUSB1+JUAB2



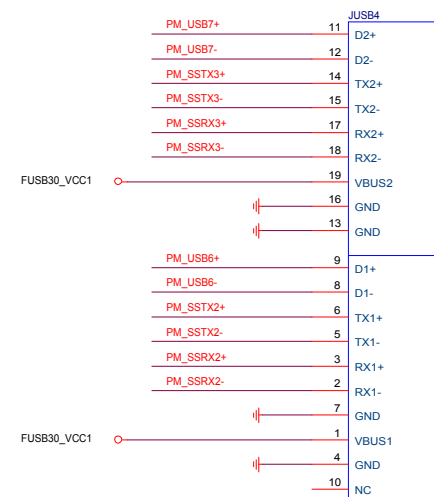
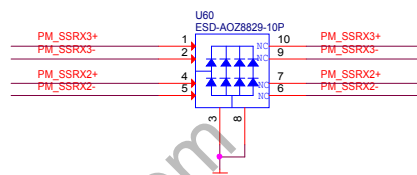
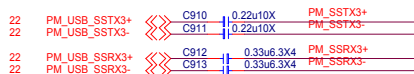
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USB 3.0-JUSB4

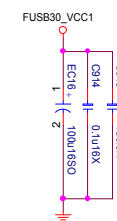
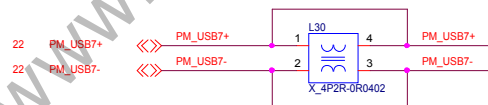
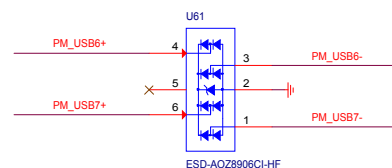
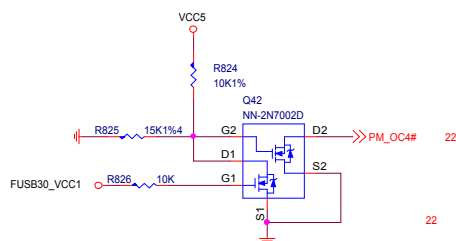


JUSB4

1.8A



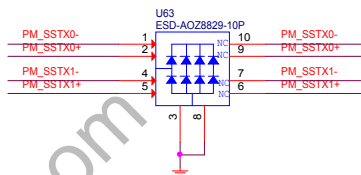
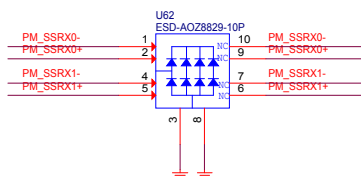
EX10 CONNECTOR
 BH2X10(20#-2PITCH_BLACK-RH-4
N32-2101731-AO3



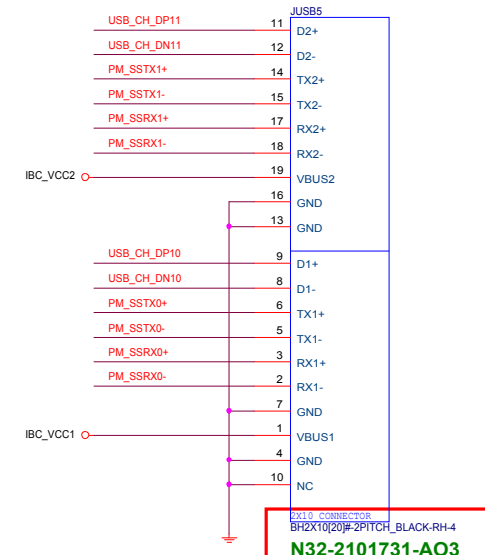
USB 3.0-JUSB5 With Charge(BC1.2)

JUSB5

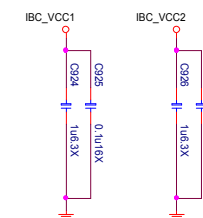
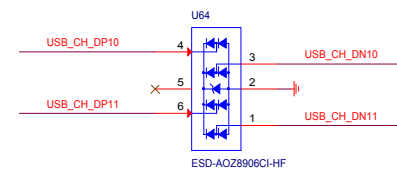
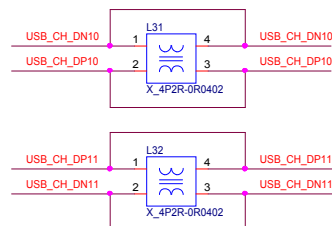
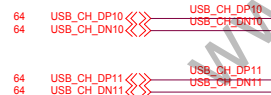
1.7A+1.7A



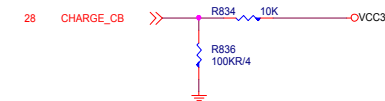
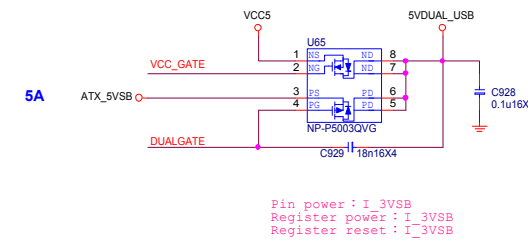
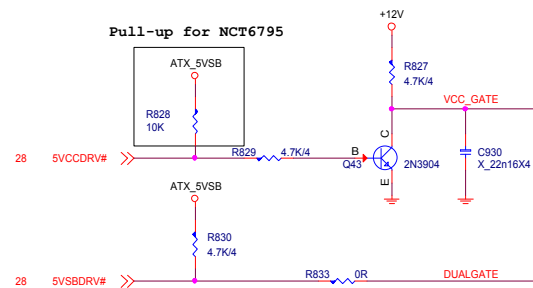
USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL



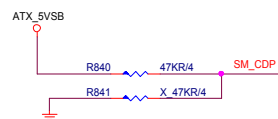
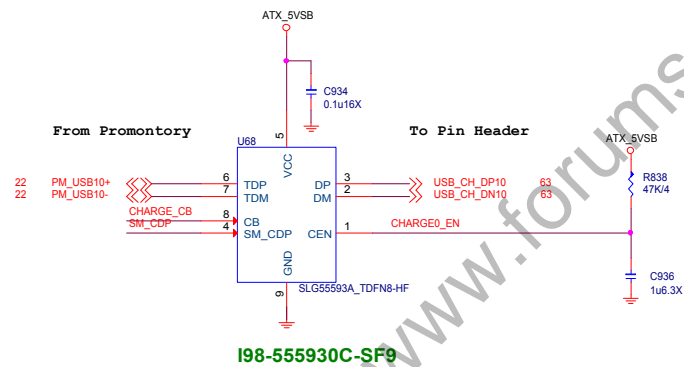
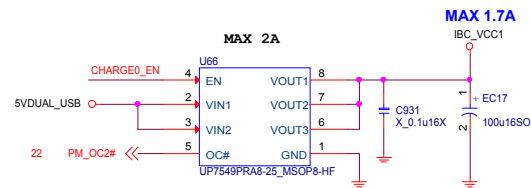
EX10 CONNECTOR
BHZXT10[20]#2PITCH_BLACK-RH-4
N32-2101731-AO3



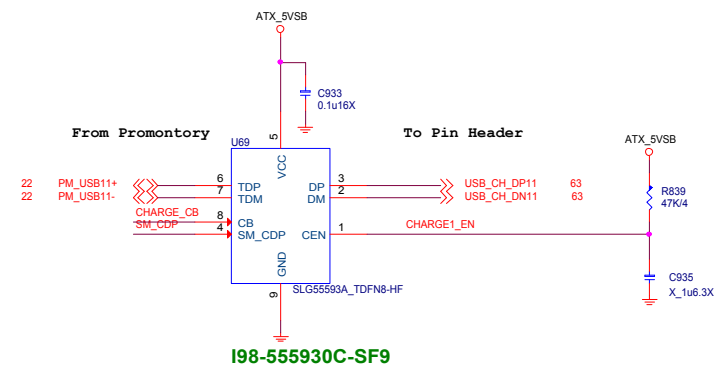
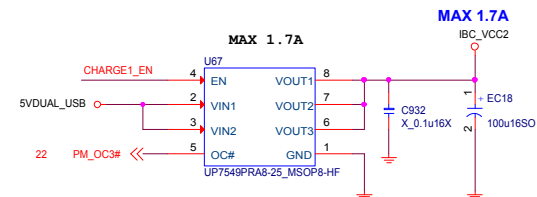
5VDUAL_USB



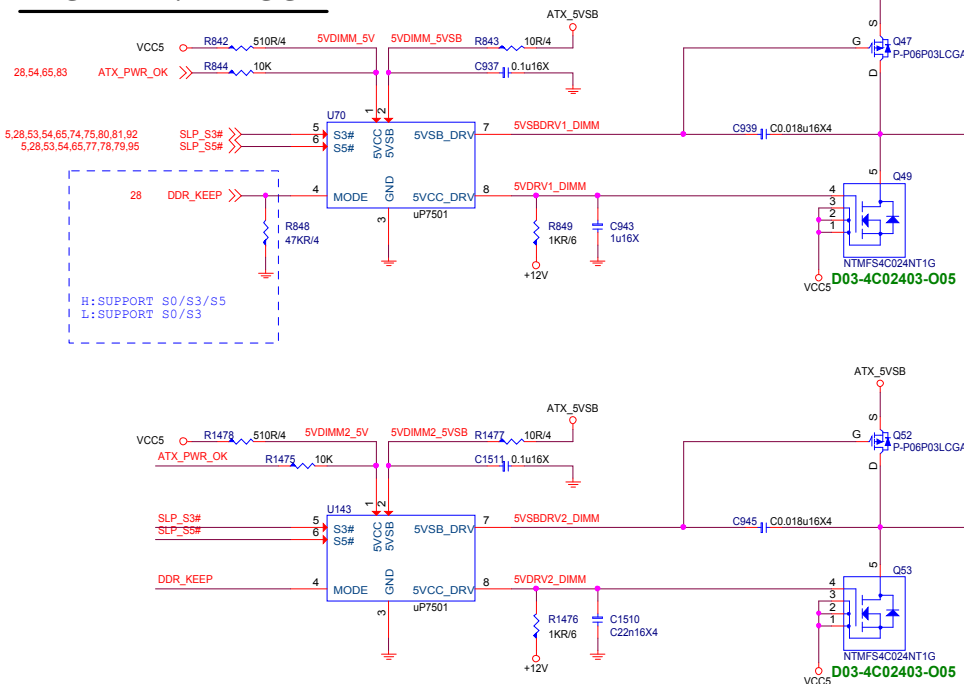
USB POWER PORT 0 For USB Charging



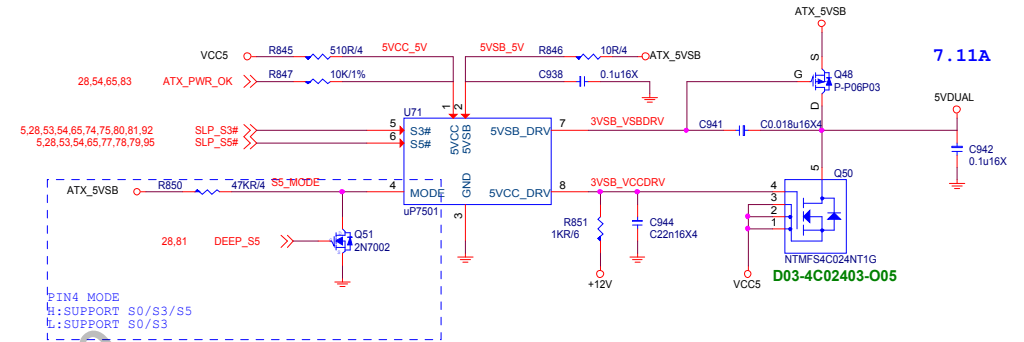
USB POWER PORT 1 For USB Charging



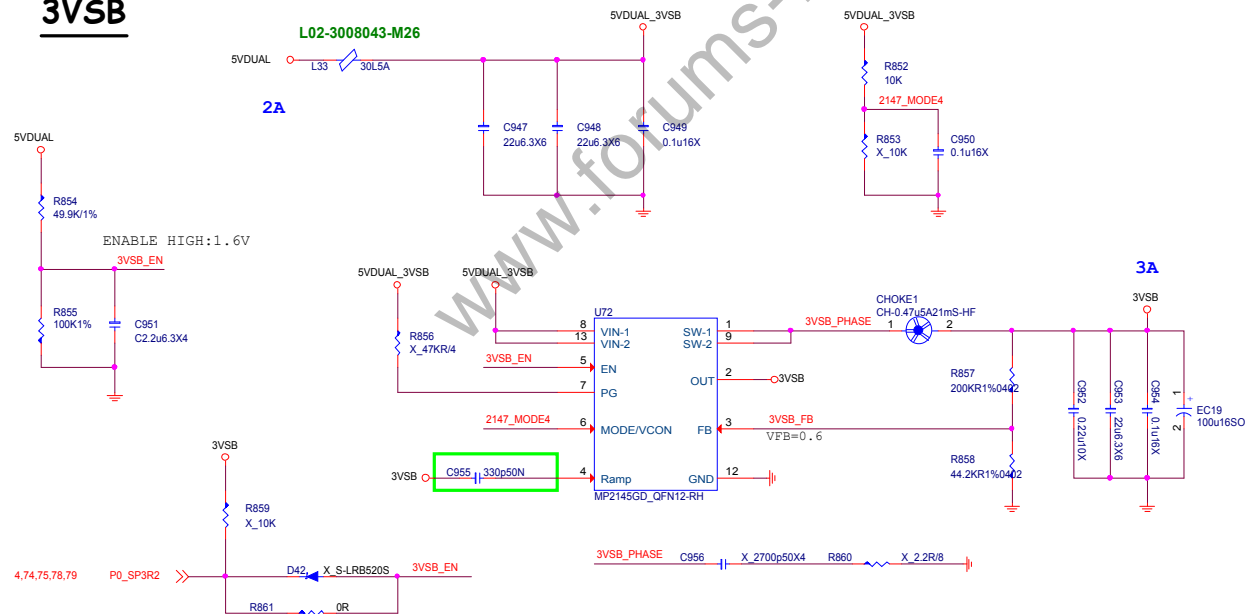
5VDIMM FOR DDR



5VDUAL For 3VSB、CPU 1.8V

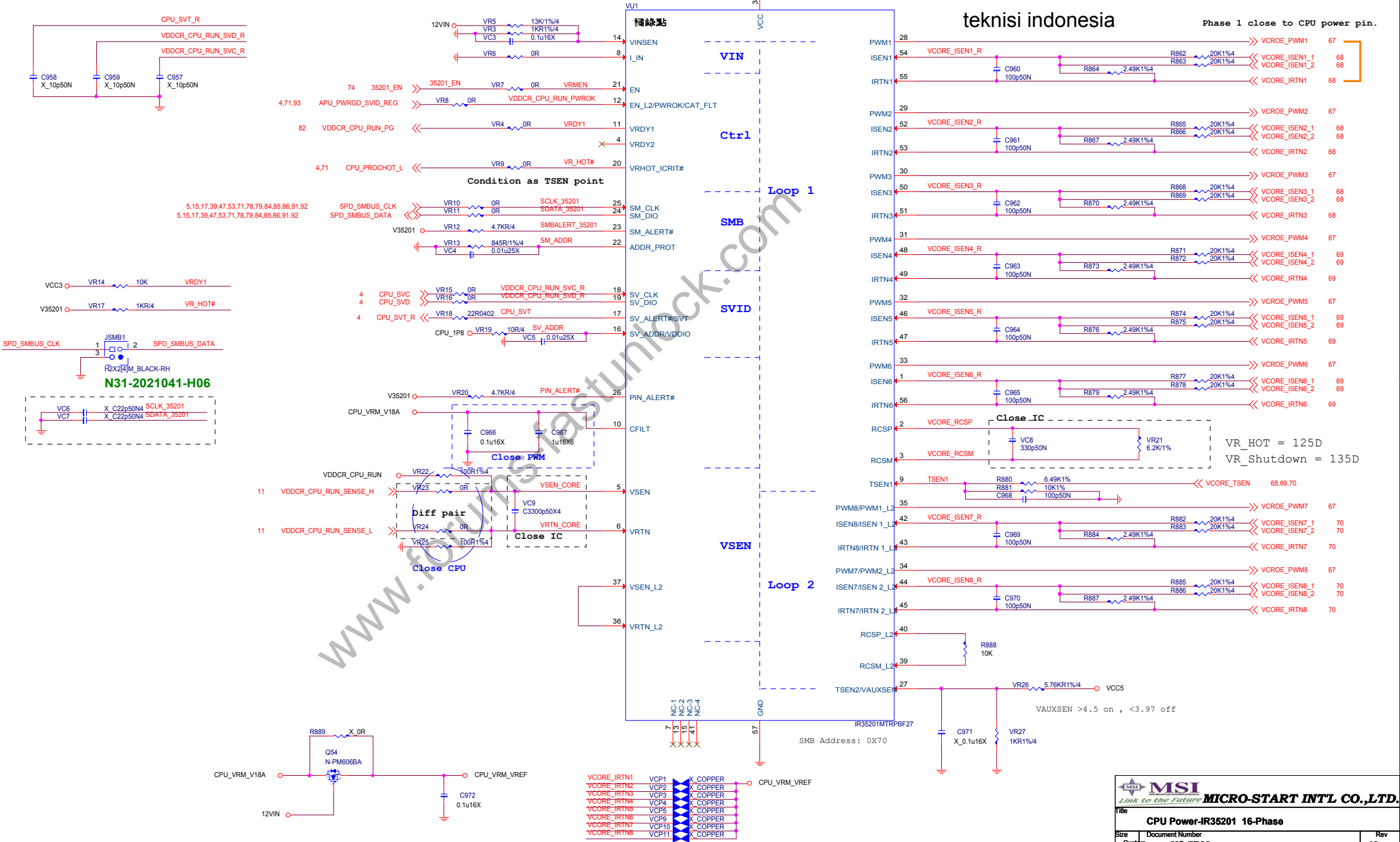


3VSB



		BOOT VOLTAGE
SVC	SVD	Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

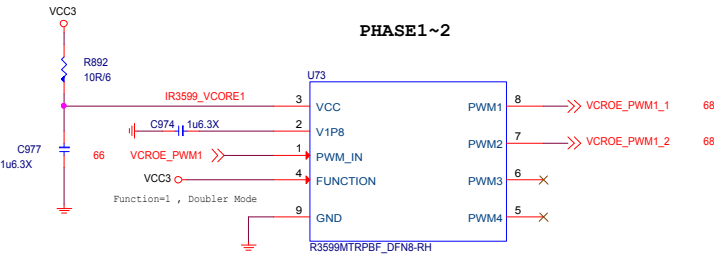
Vcore: ICC Max 255A(Group-C EDC 300A)
LL: 0.3 mohm
Total OCP: 640A(Per Phase OCP=40A)
Vcore 8+0 (Extender 16-Phase)



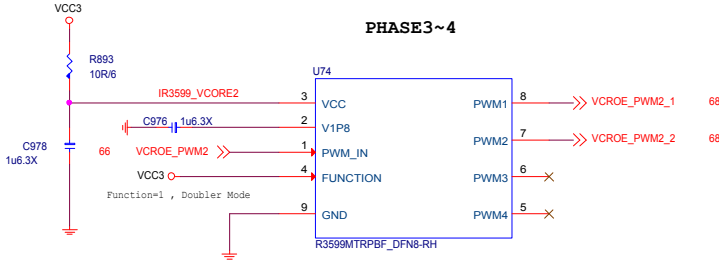
CPU_CORE Driver IC

VCORE Double 16-PHASE

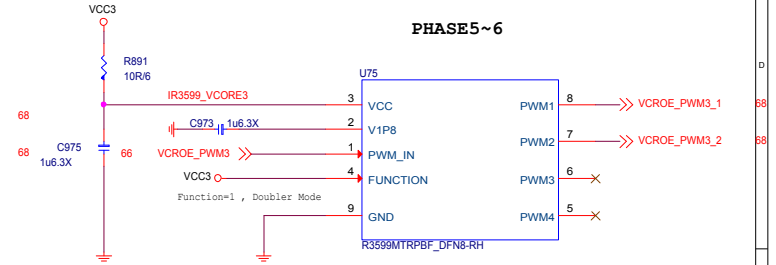
PHASE1~2



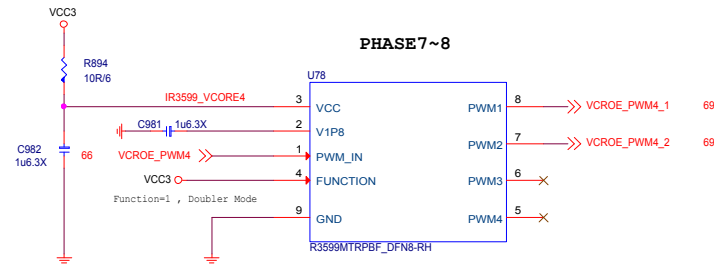
PHASE3~4



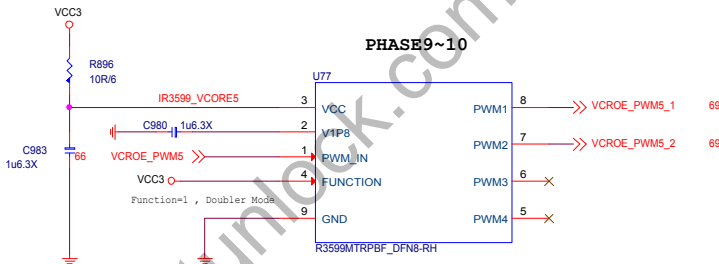
PHASE5~6



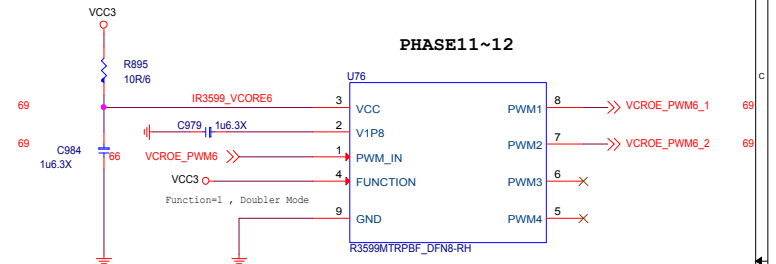
PHASE7~8



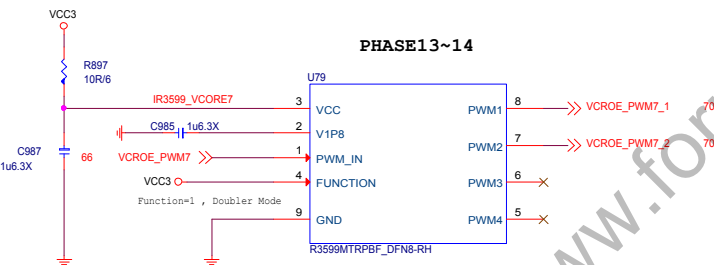
PHASE9~10



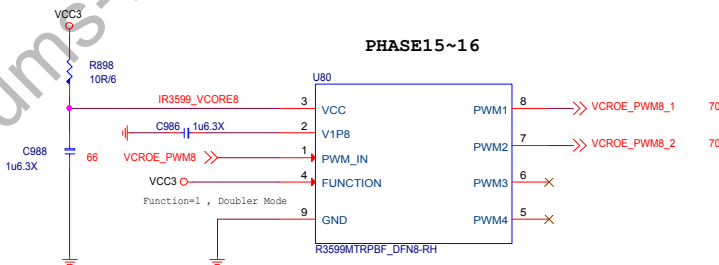
PHASE11~12

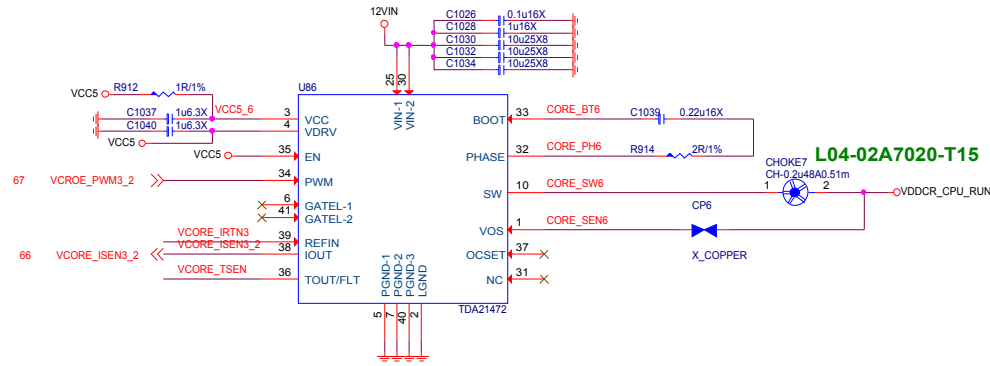
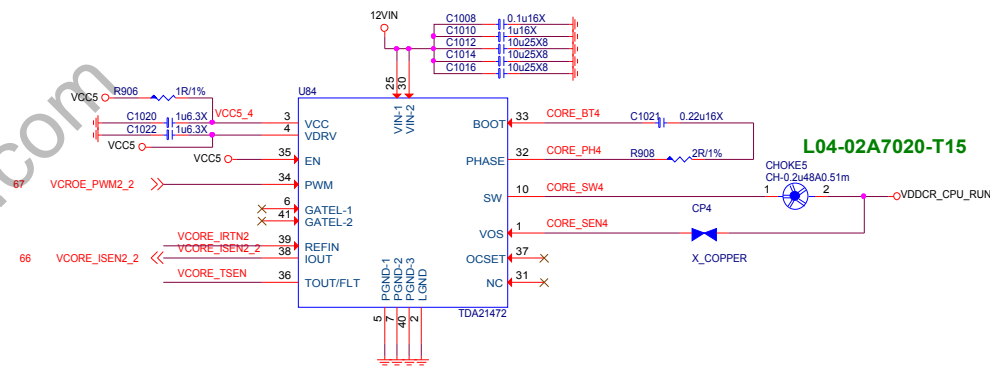
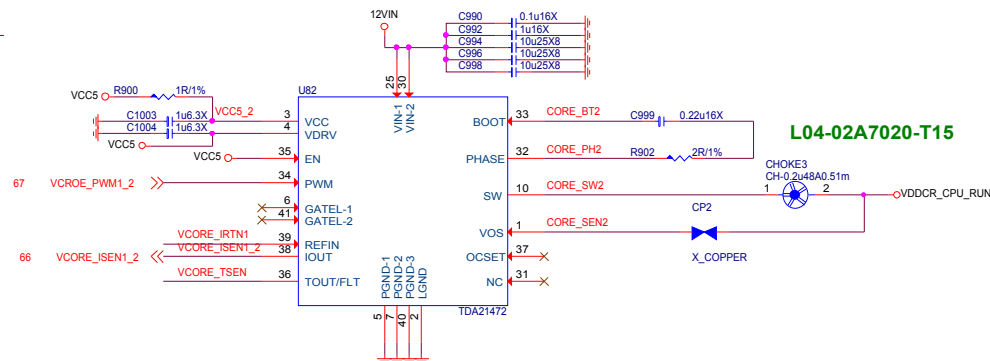


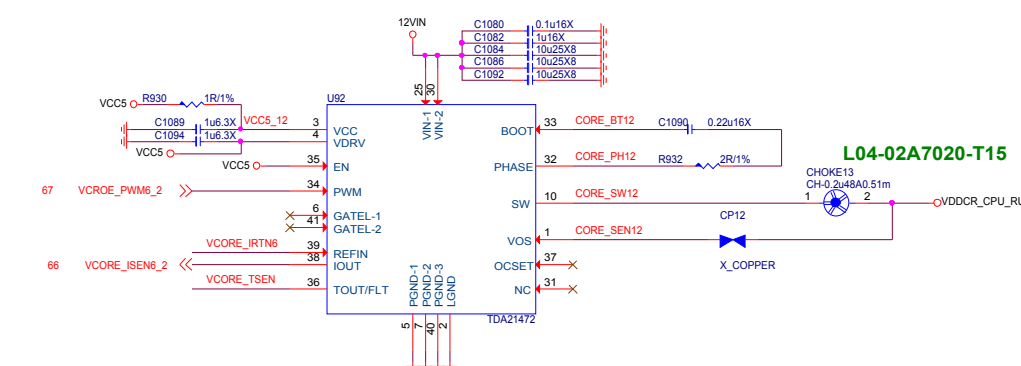
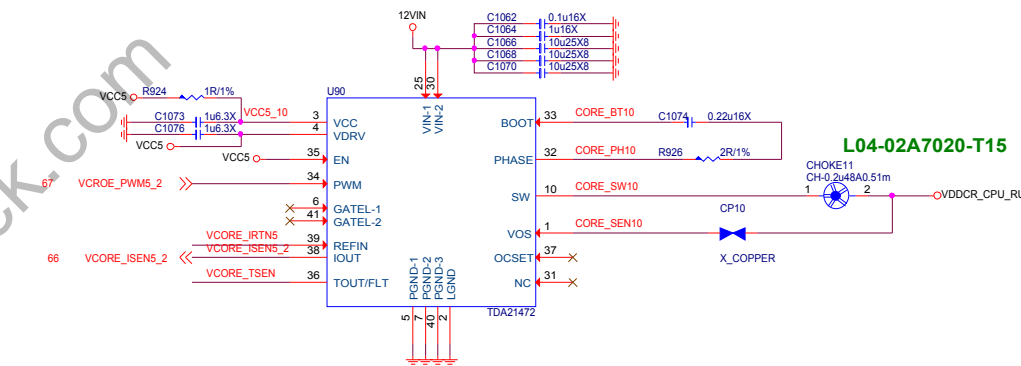
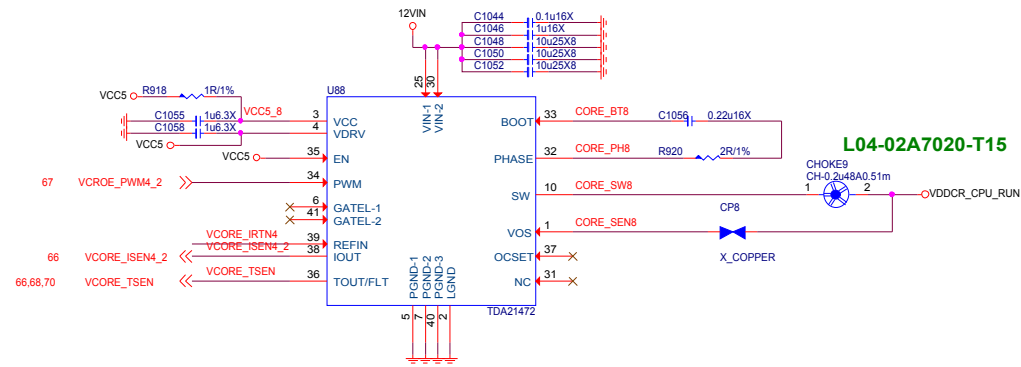
PHASE13~14

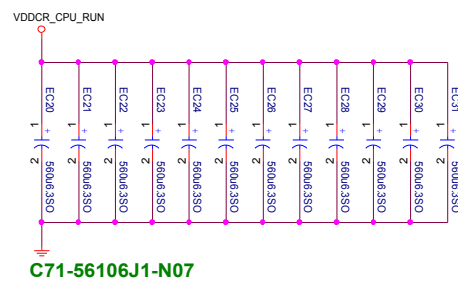
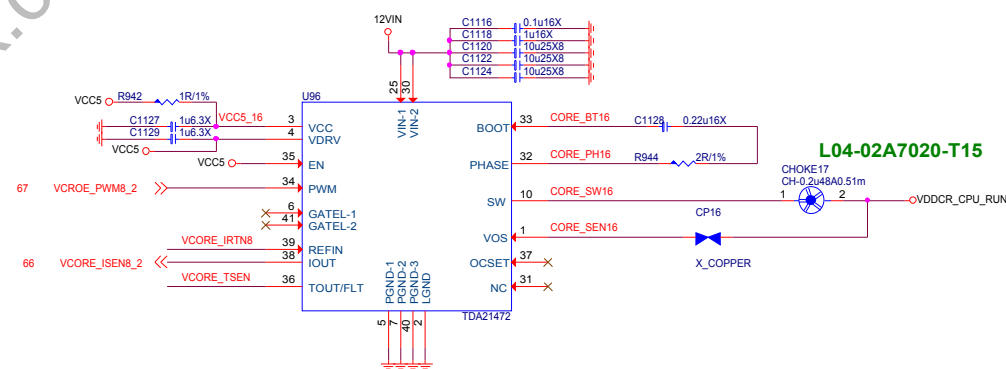
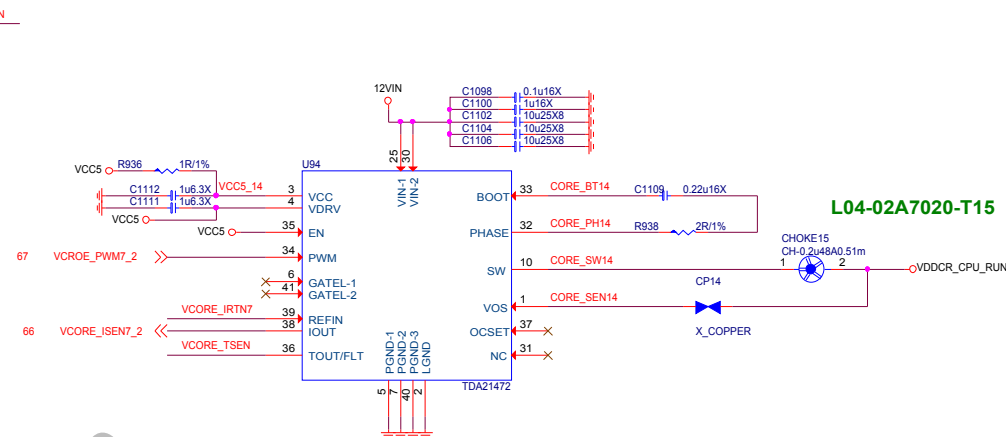


PHASE15~16



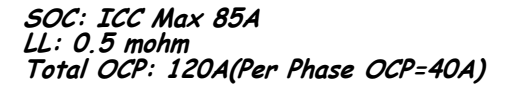






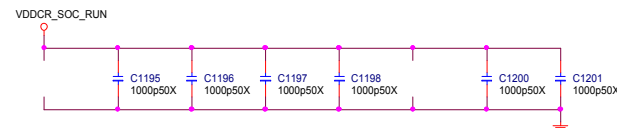
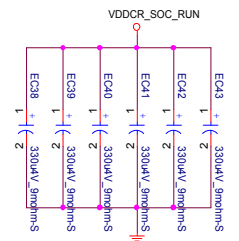
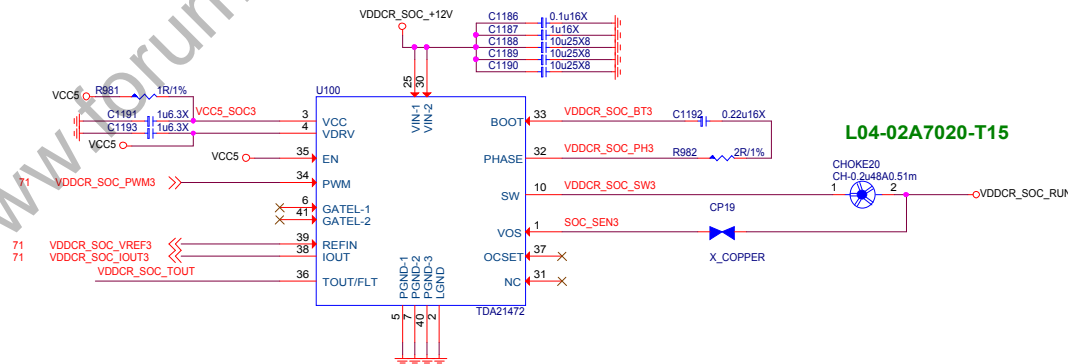
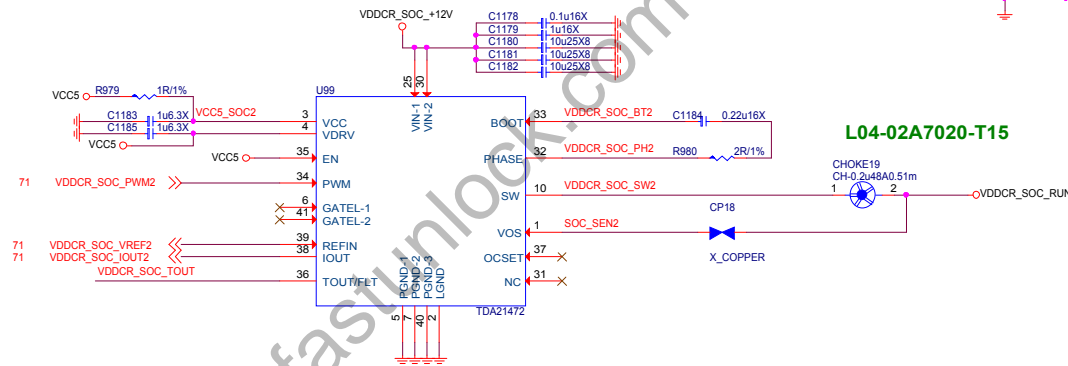
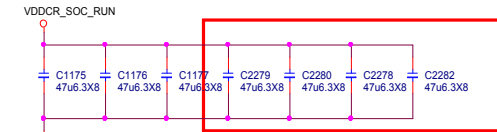
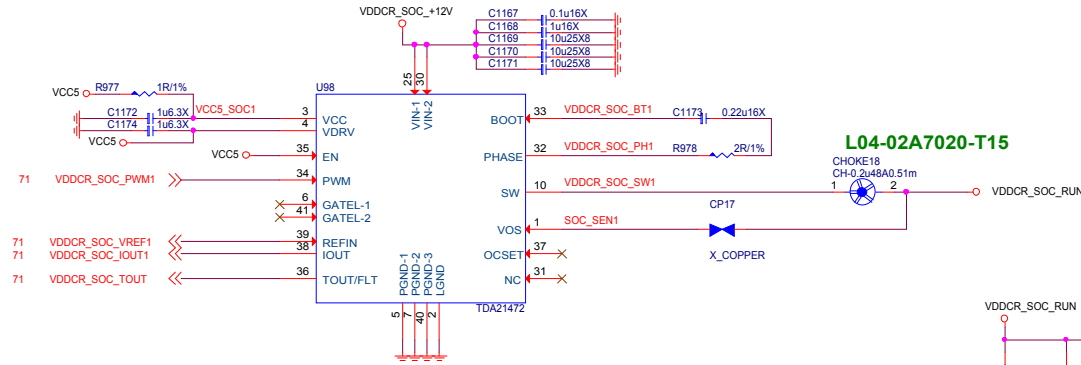
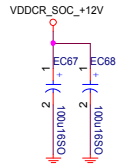
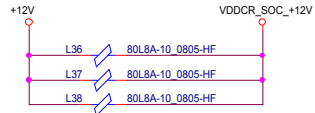
80A
OCP=120A

		BOOT VOLTAGE
SVC	SVD	Pre PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

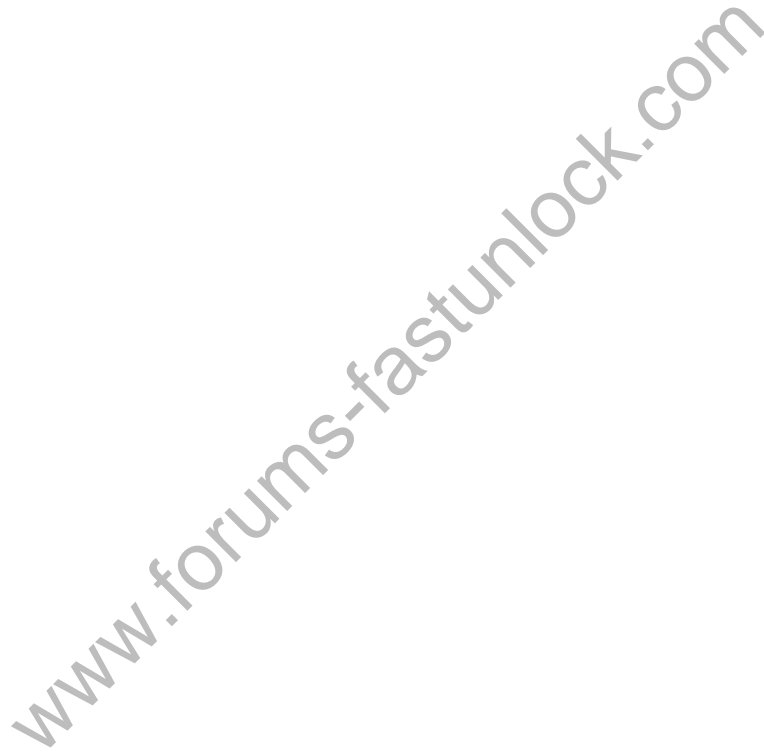


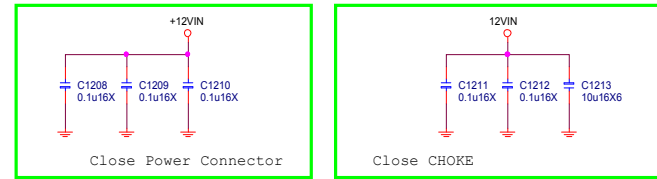
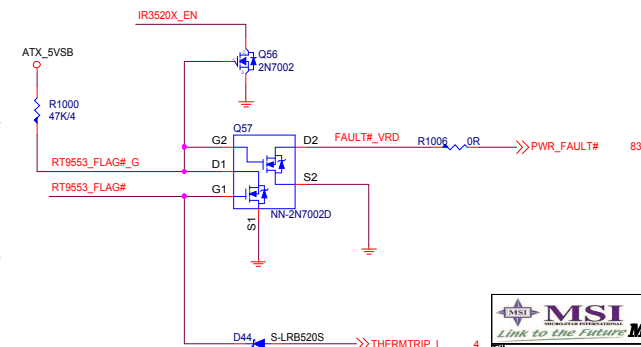
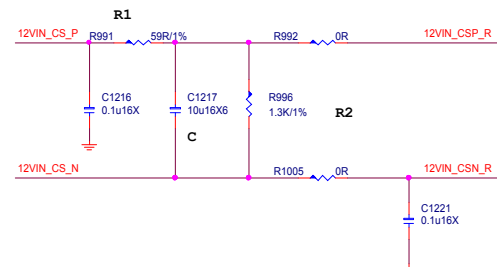
CPU_SOC Driver+MOS IC

3-PHASE

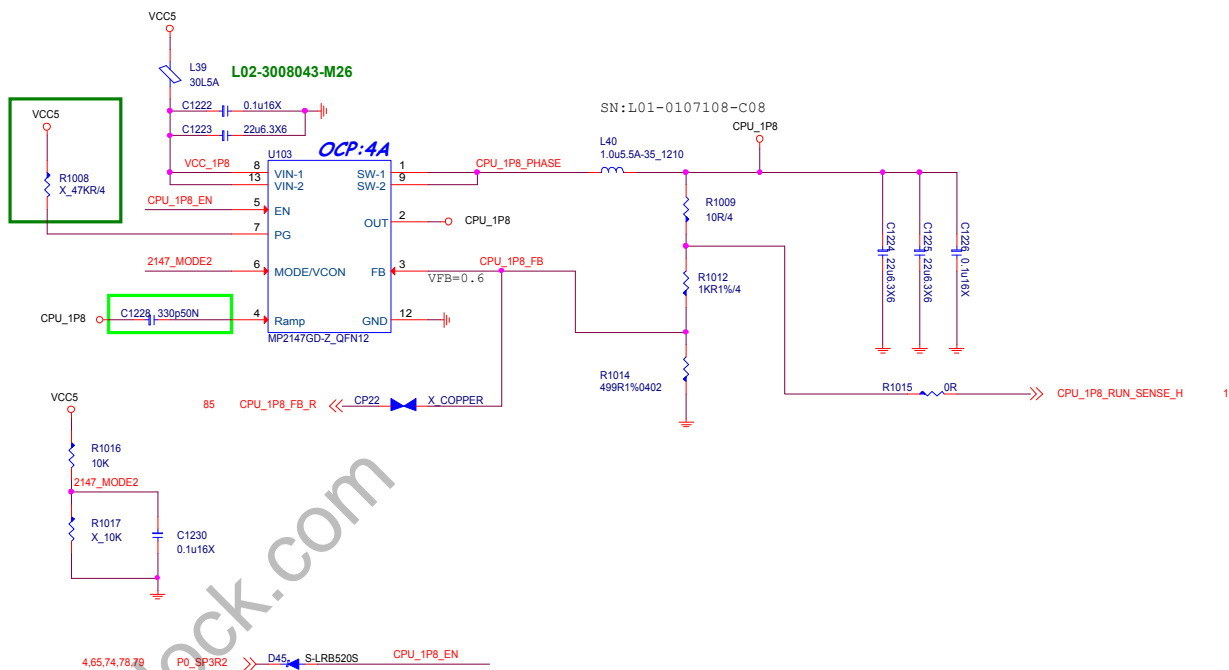
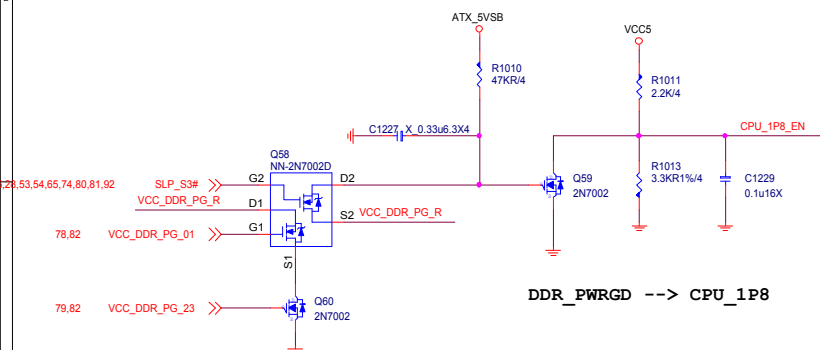


2A

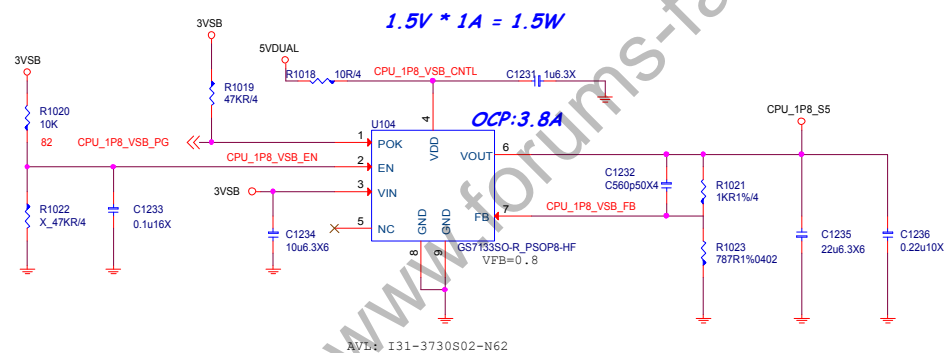


$$I_{\text{ripple}} = 5.6A$$
[illegible]
$$\Delta I_{sense} = 228\text{mV} / 100 * 0.39\text{m} = 5.846\text{A}$$


3A



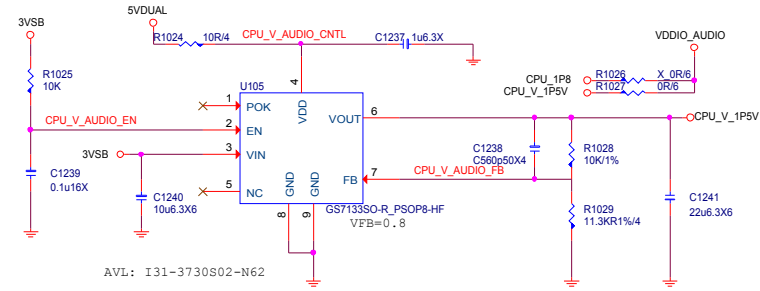
1A



VDDIO_AUDIO Circuit

1.5V
0.25A

$$1.8V * 0.25A = 0.45W$$

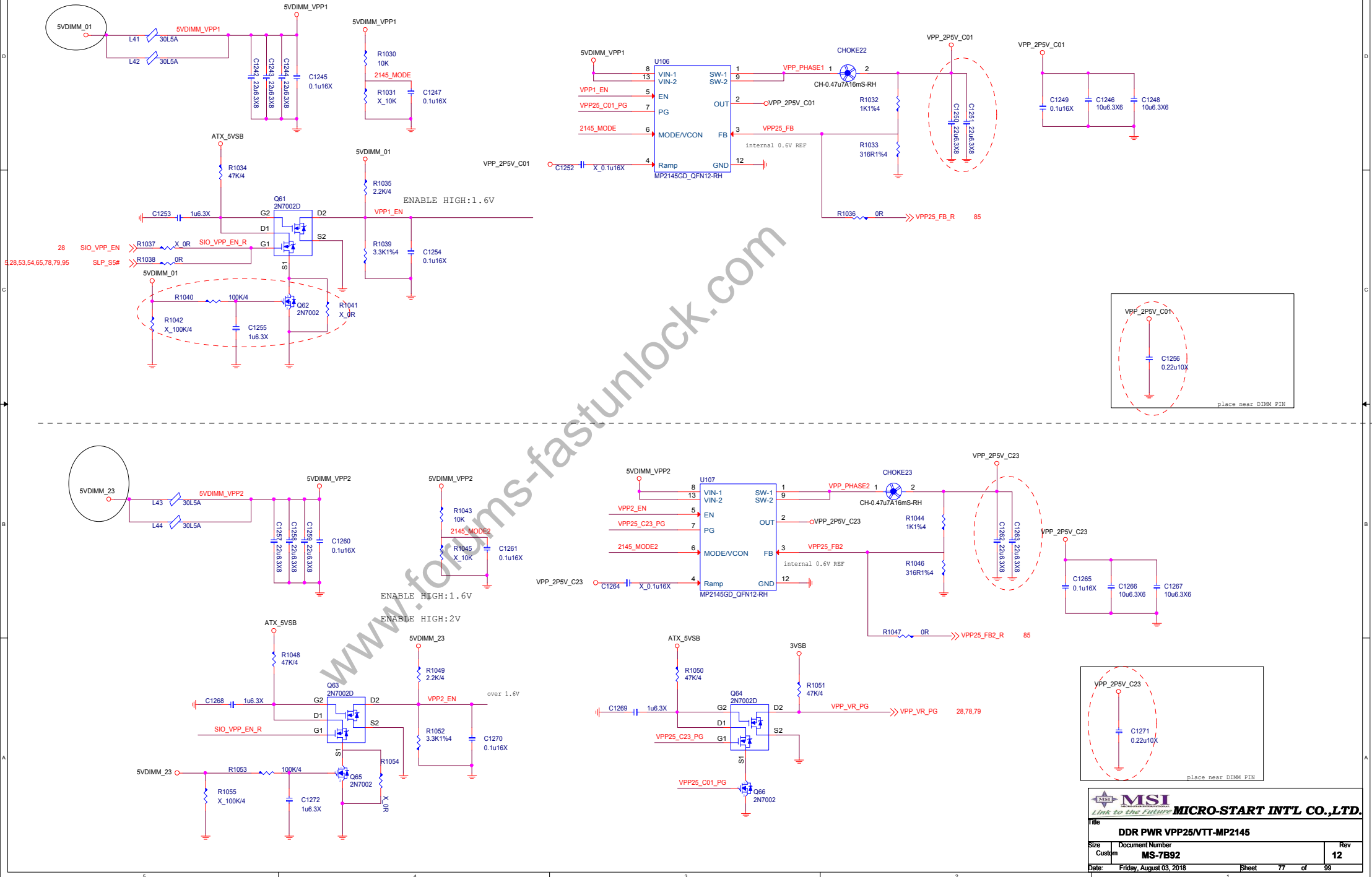


AVL: I31-3730S02-N62

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4DIMM :2.24A FOR DDR VPP2.5V

2.5V±0.25V-0.125V
JE3D79 DDR4 max 3V



DDR Power1-PV4210-2-Phase

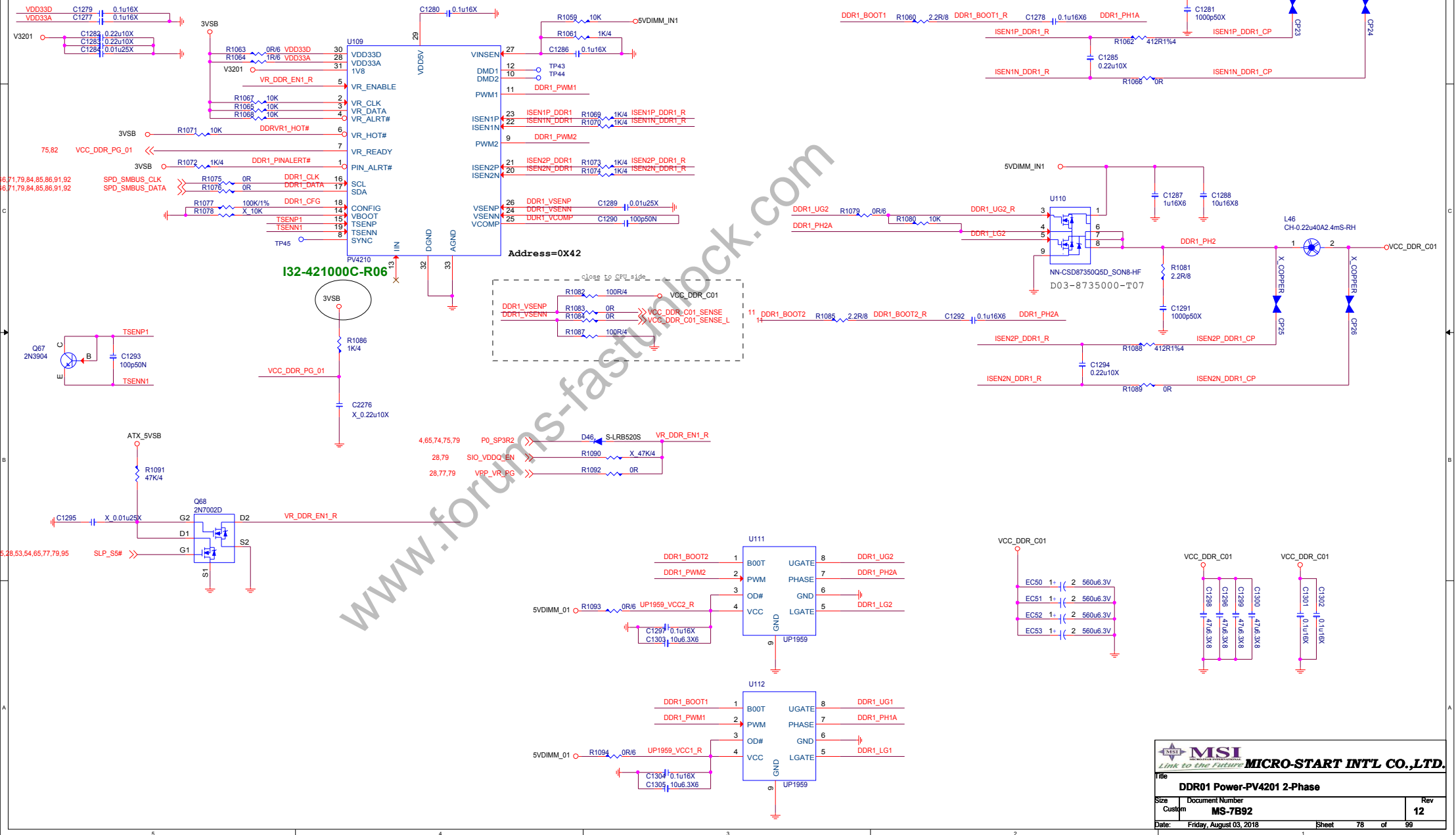
DDR4_1.2V 15A+9.5A+1.2A=26A

15A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

OCp: 50A



DDR4_1.2V 15A+9.5A+1.2A=26A
15A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT
OCP: 50A

5V DIMM_23

CHOKES25

CH-0.47u22A2.2mS-HF

5V DIMM_IN2

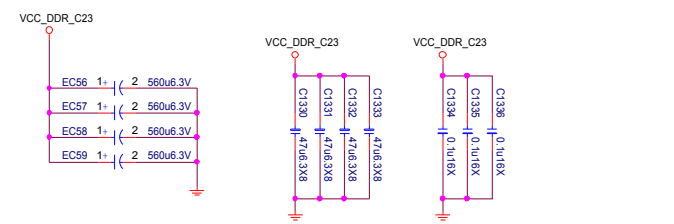
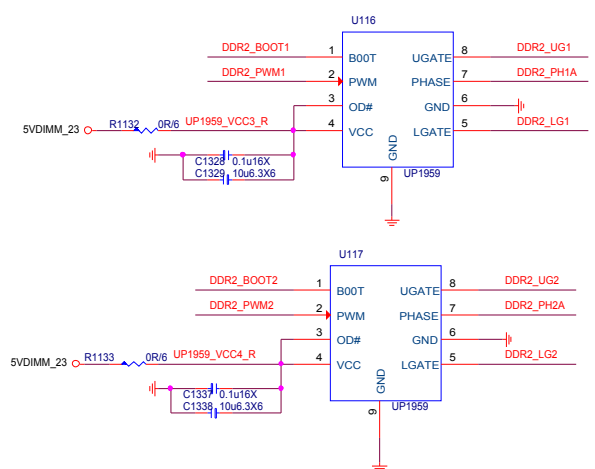
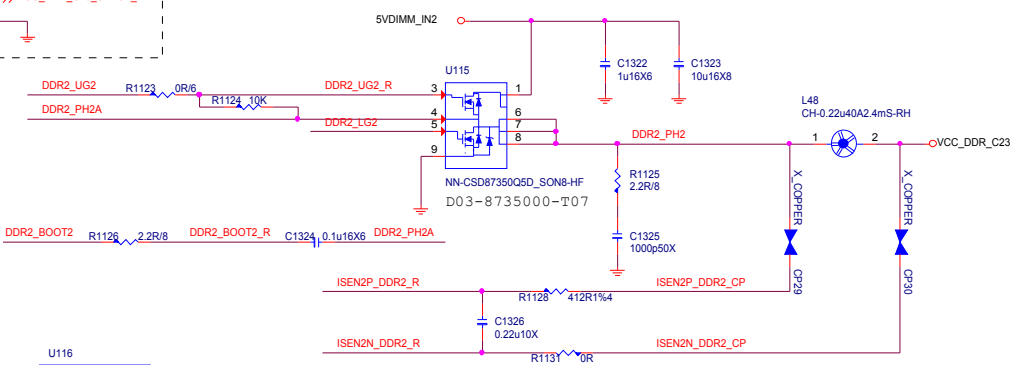
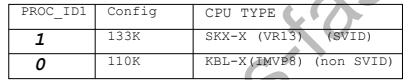
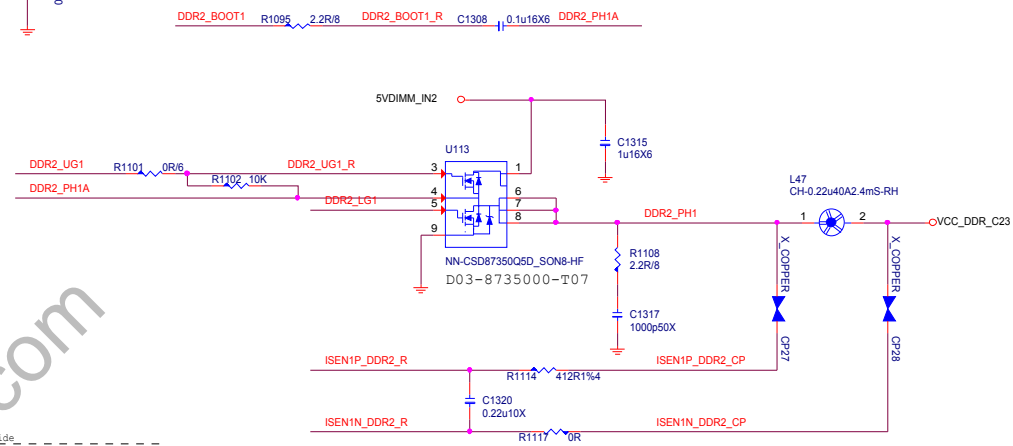
5V DIMM_IN1

C1306 0.1u16X

EC54

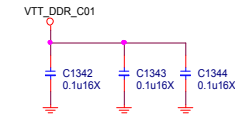
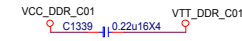
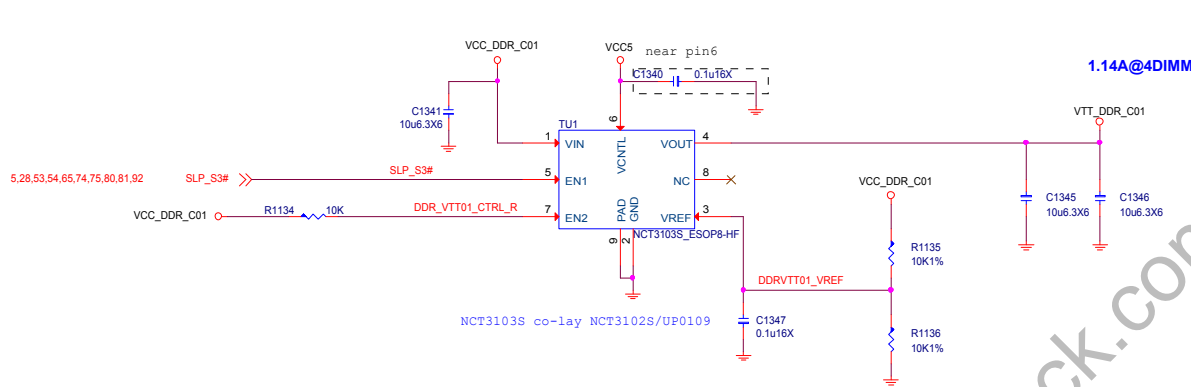
EC55

C1307 0.1u16X



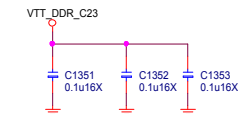
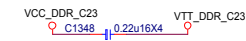
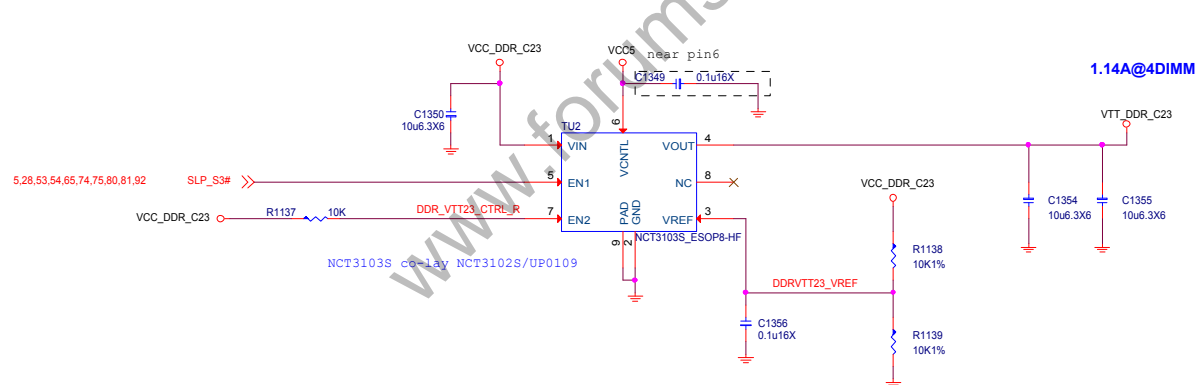
DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



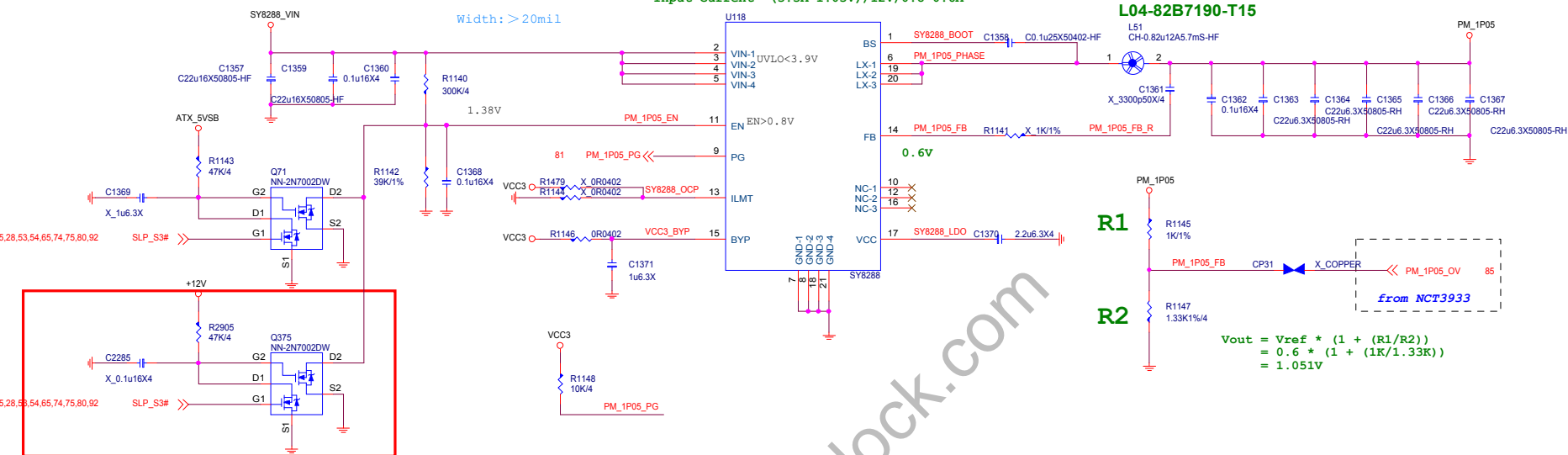
DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



FOR Promontory 1.05V_S0

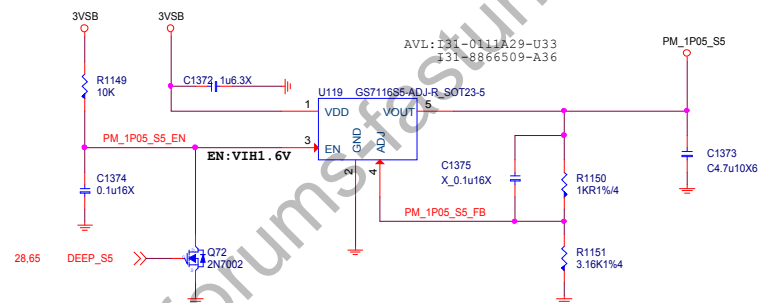
1.05V
S0:5.5A
S5:0.05A



SY8288_OCP	OCP
0	8A
floating	12A
1	16A

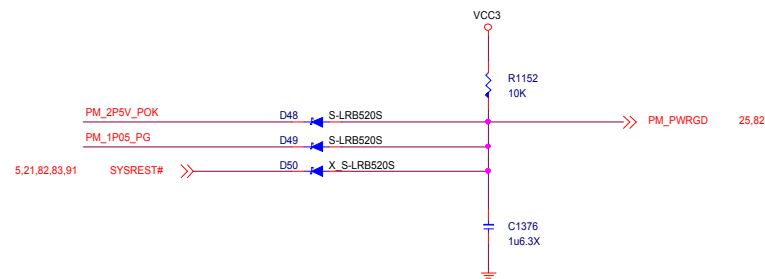
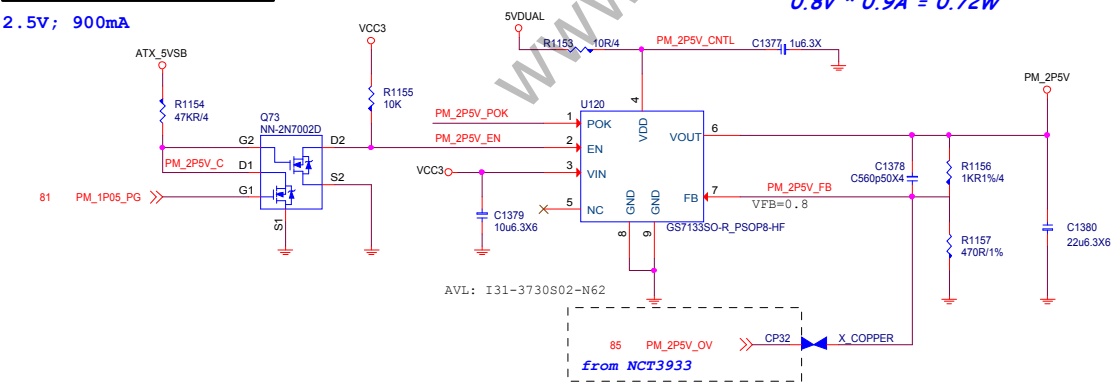
FOR Promontory 1.05V_S5

0.05A



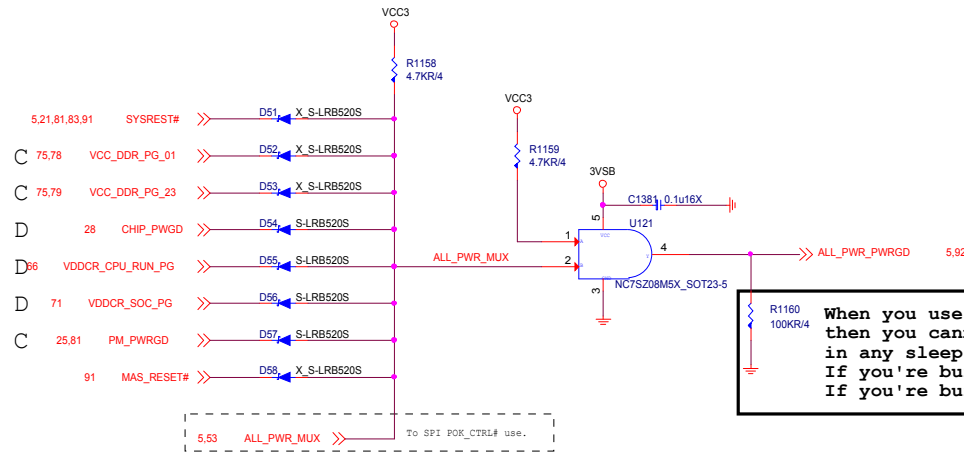
Promontory-2.5V

2.5V; 900mA



ALL POWER GOOD MUX

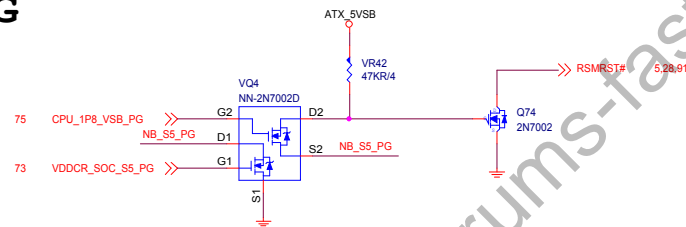
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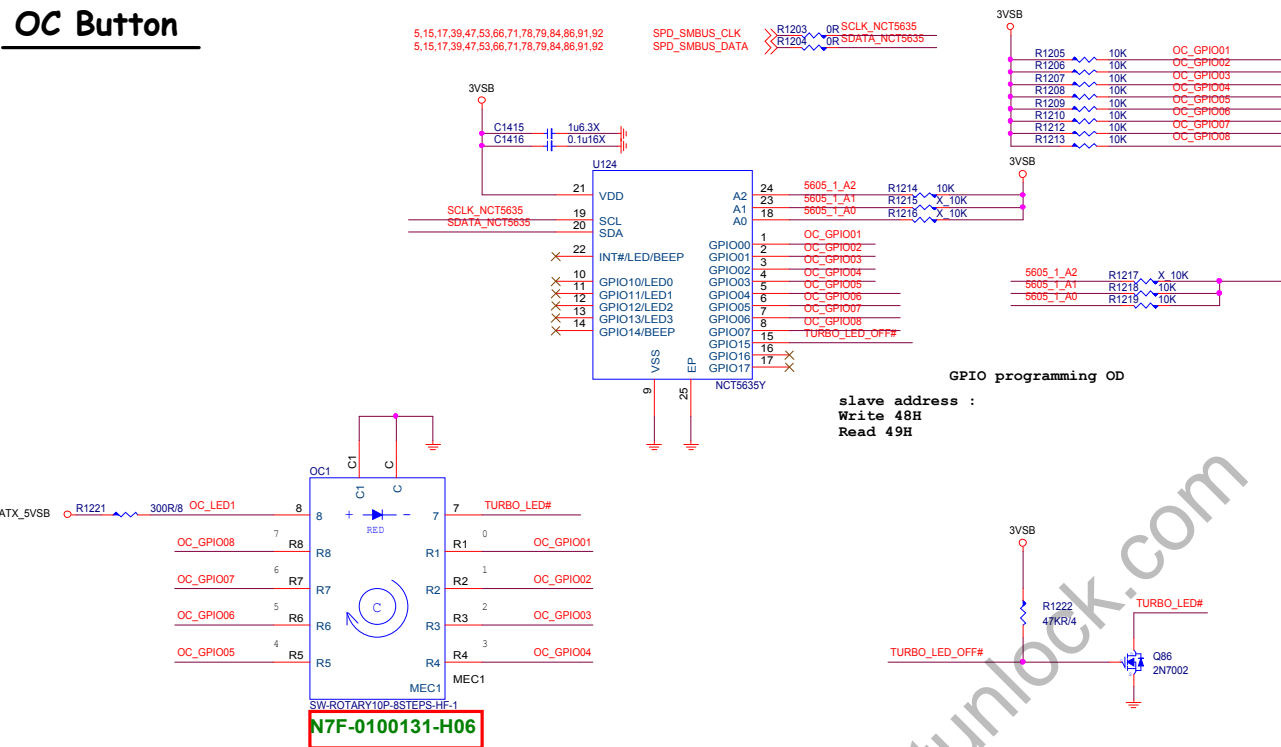
When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

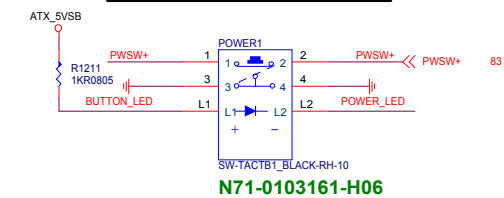
S5 PG



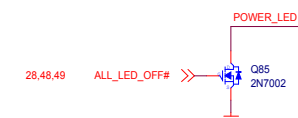
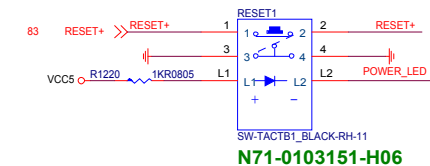
OC Button



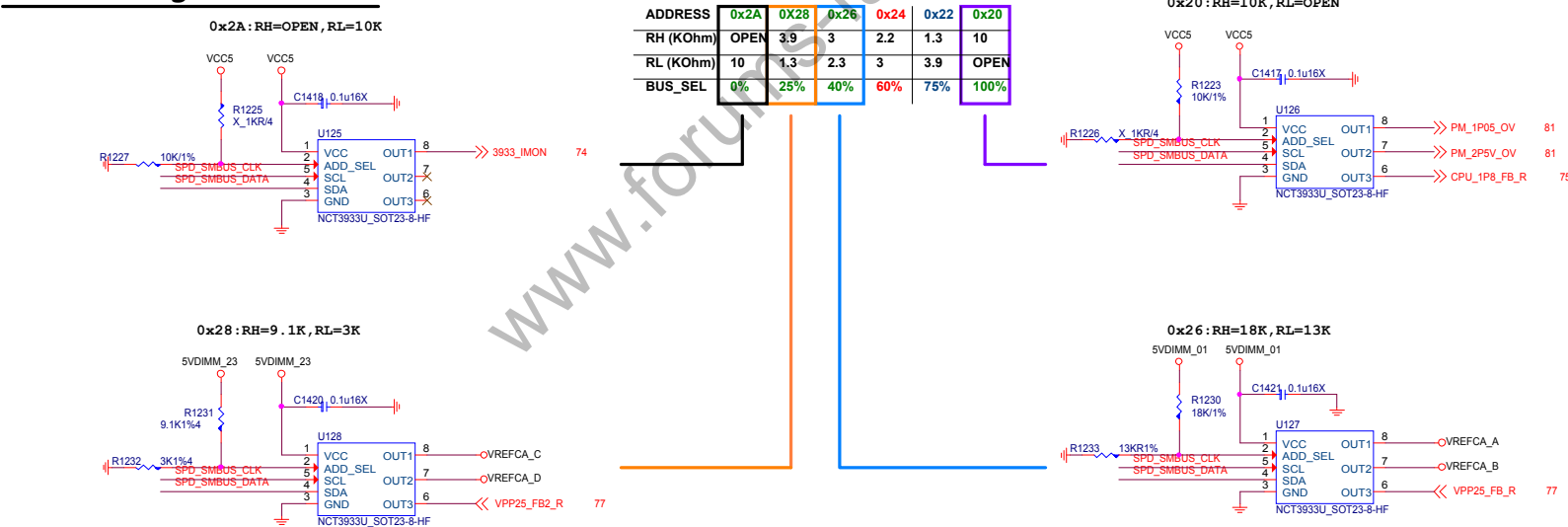
Power ON Button



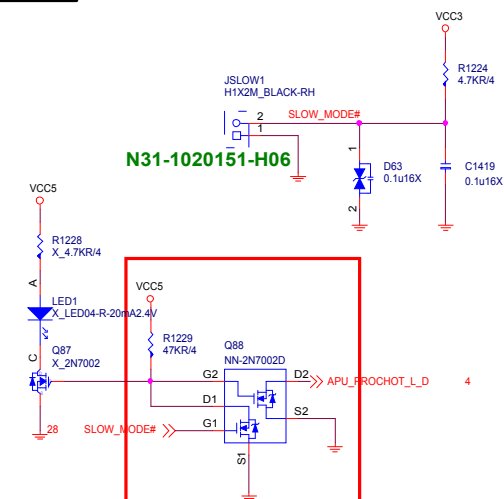
Reset Button



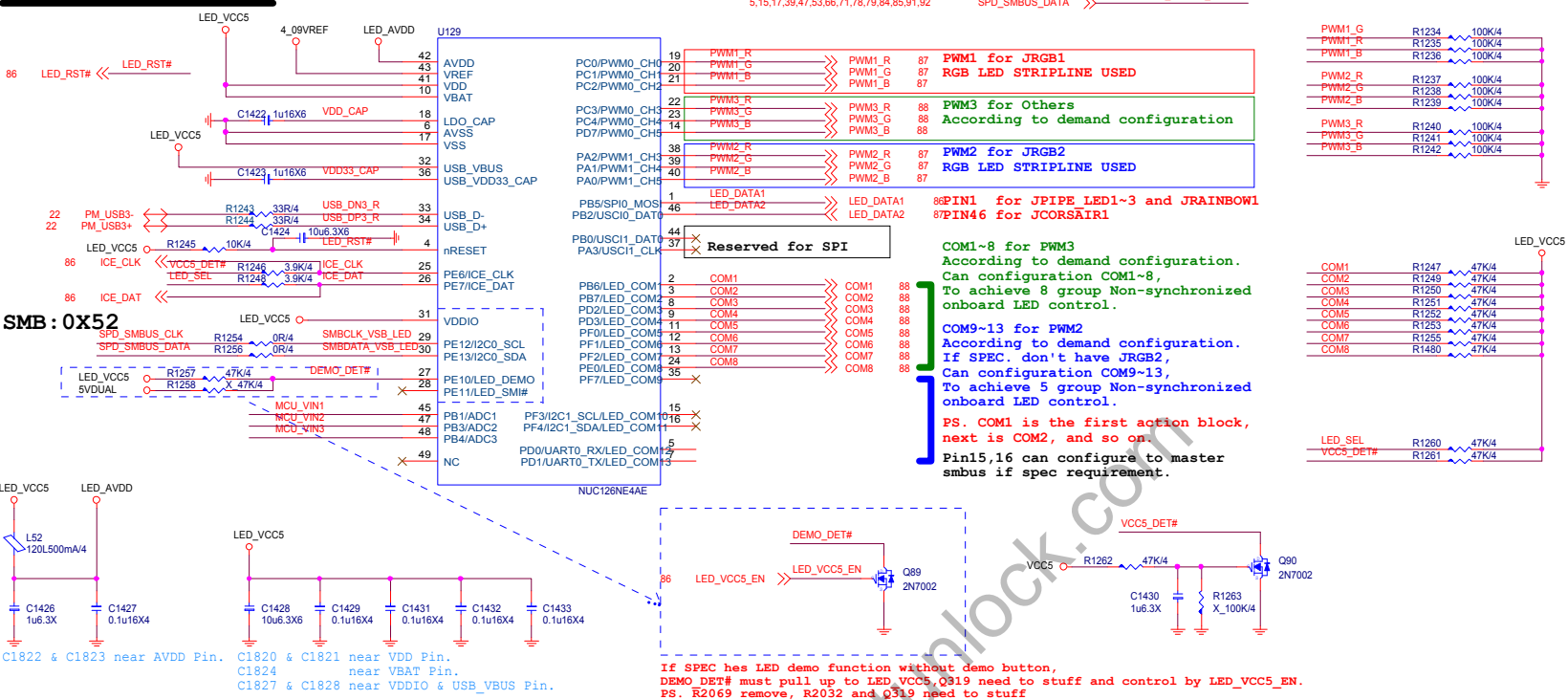
Over Voltage Control IC



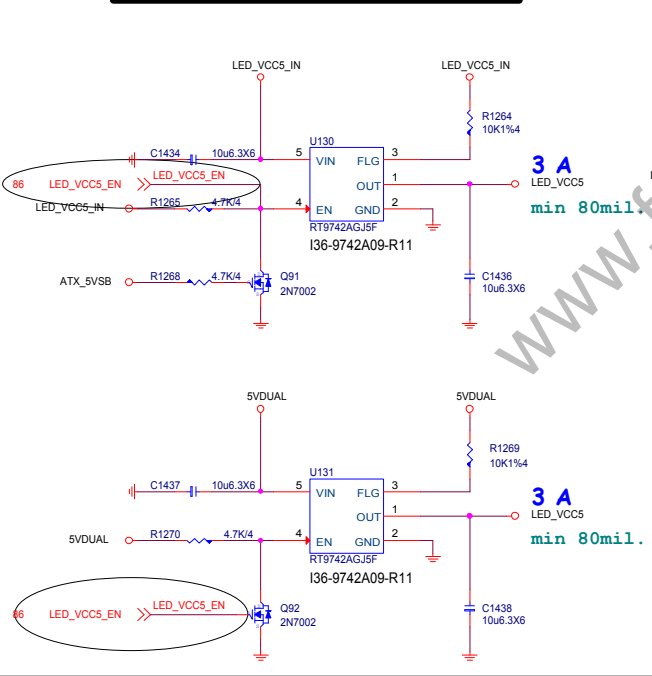
Slow Mode



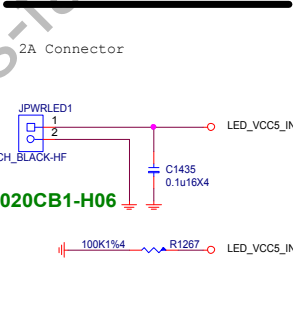
48 PIN LED MCU



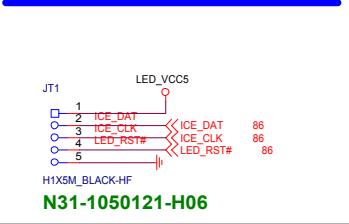
EXTERNAL POWER INPUT



External Power



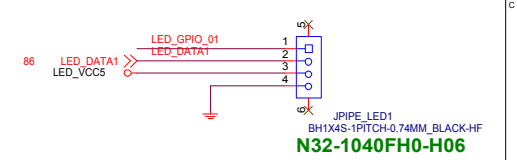
JT1 for FW update



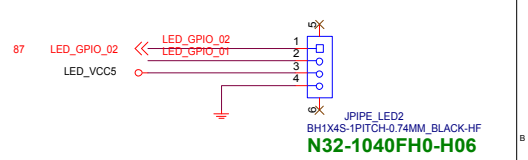
Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

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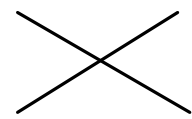
1 PCH HEATSINK LED
PCS LED*0.16W=W



2 AUDIO/IO Cover LED
PCS LED*0.16W=W

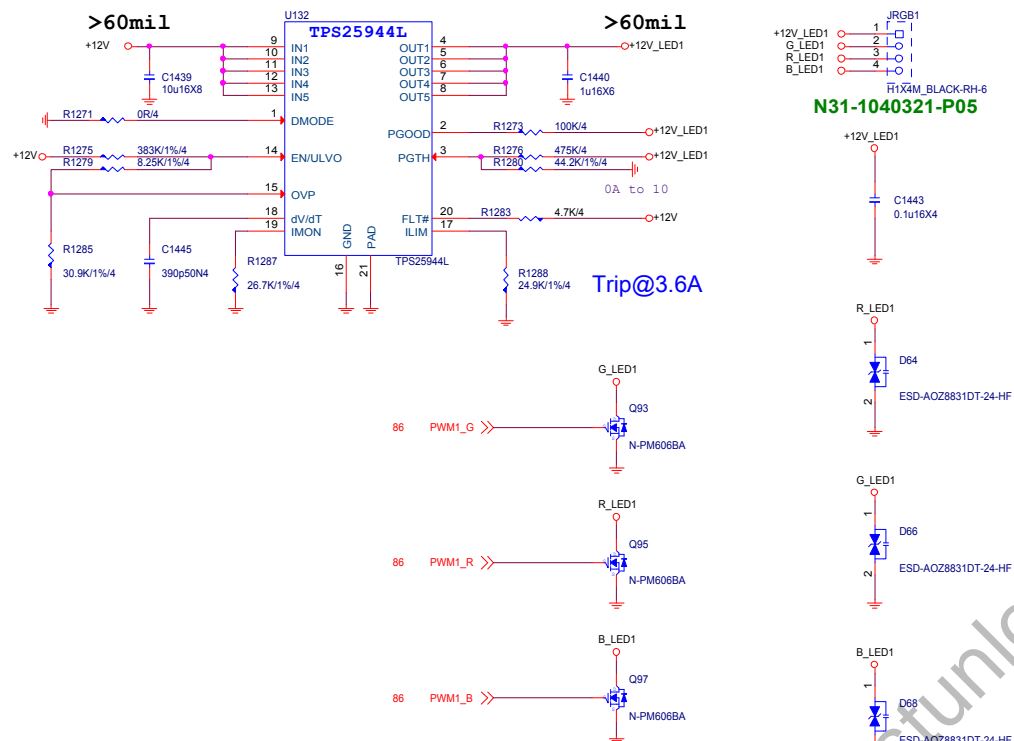


3 MOS HEATSINK LED
PCS LED*0.16W=W

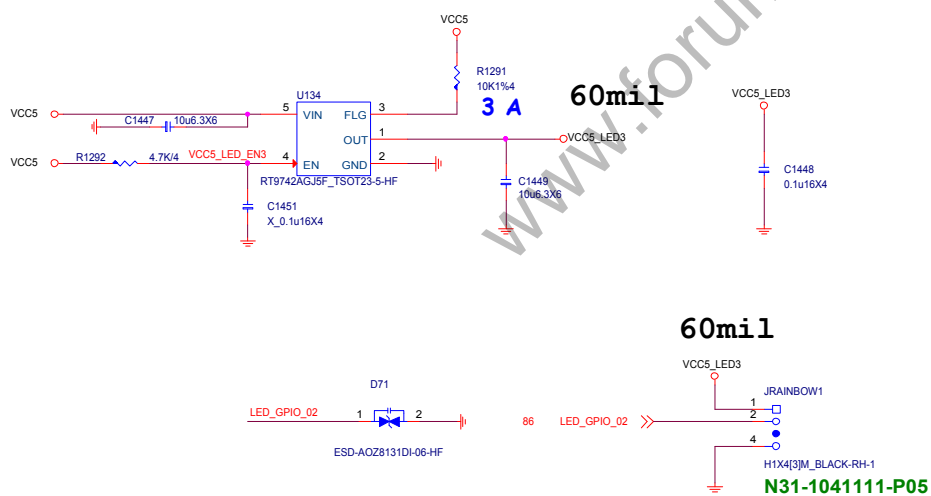


JPIPE:PIN1:output ,PIN2:input
PIN2:MCU IN
PIN1:HEATSINK OUT

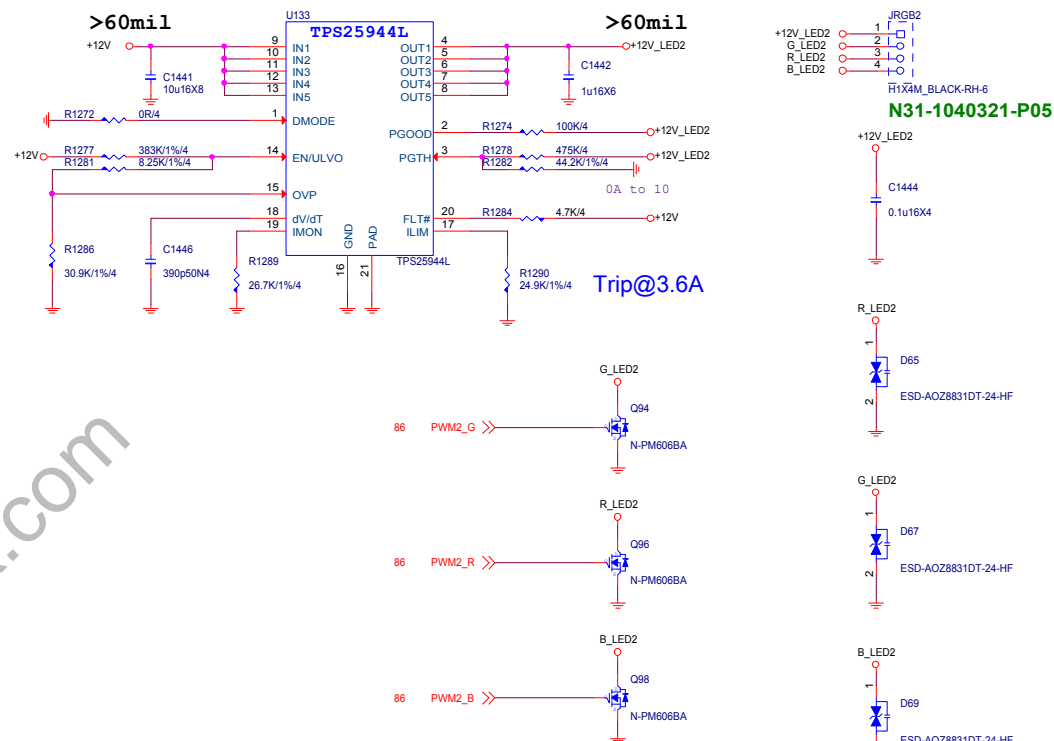
JRGB1



----- 外接LED 燈條 (RGB) -----
----- RGB 文字面 (JRGB1) -----
----- 手冊註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺 -----

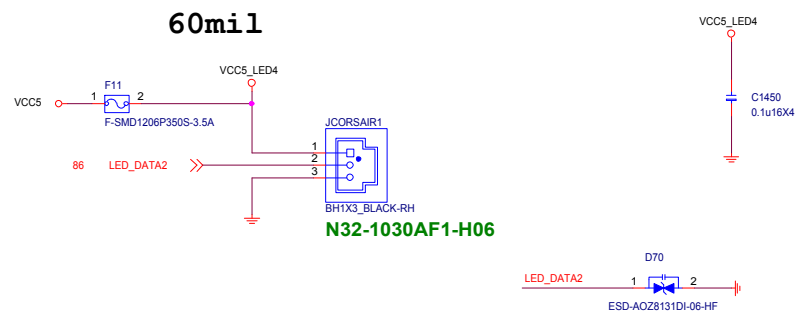
JRAINBOW1

JRGB2



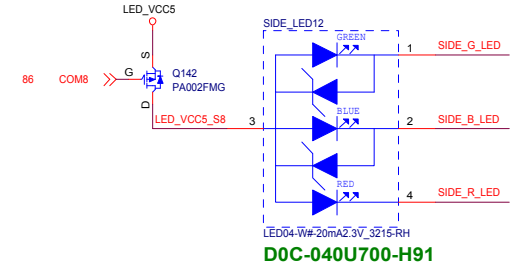
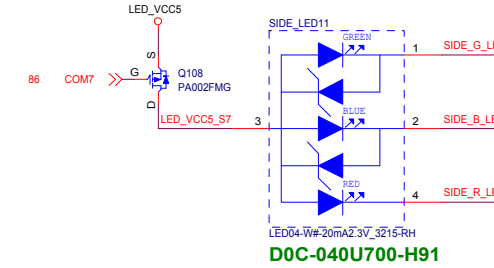
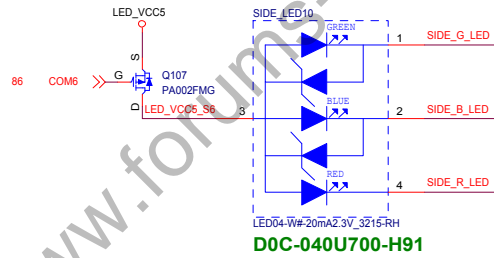
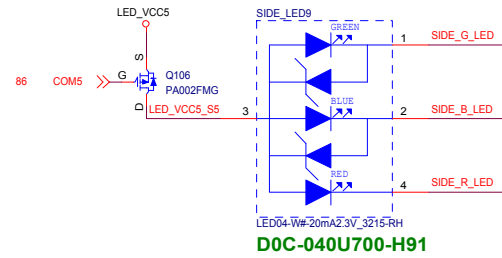
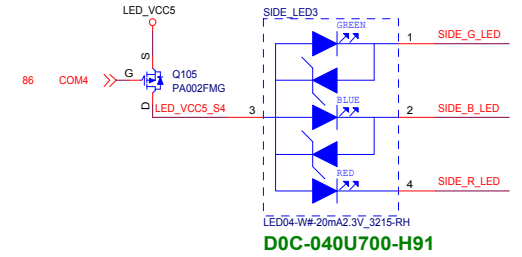
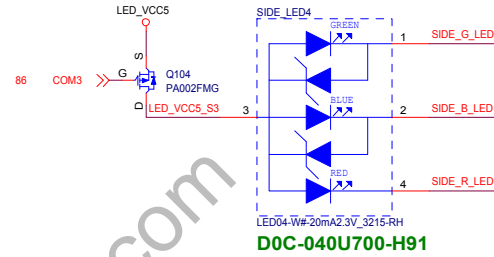
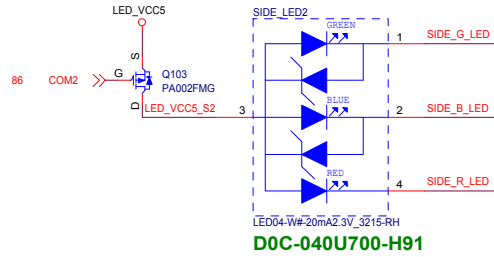
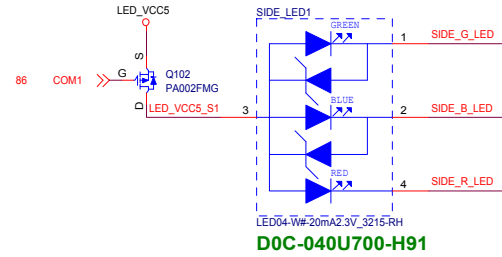
----- 外接LED 燈條 (RGB)
----- PCB 文字面 (JRGB2)
----- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) ,
----- 長度限制為2公尺

JCORSAIR1



MICRO-STAR INT'L CO.,LTD			
MS-7B92			
Size Custom	Document Description LED JRGB/JCORSAIR/JRAINBOW		Rev 12
Date: Friday, August 03, 2018		Sheet 87 of 99	

BOARD SIDE LED*8 SET
FORM MCU



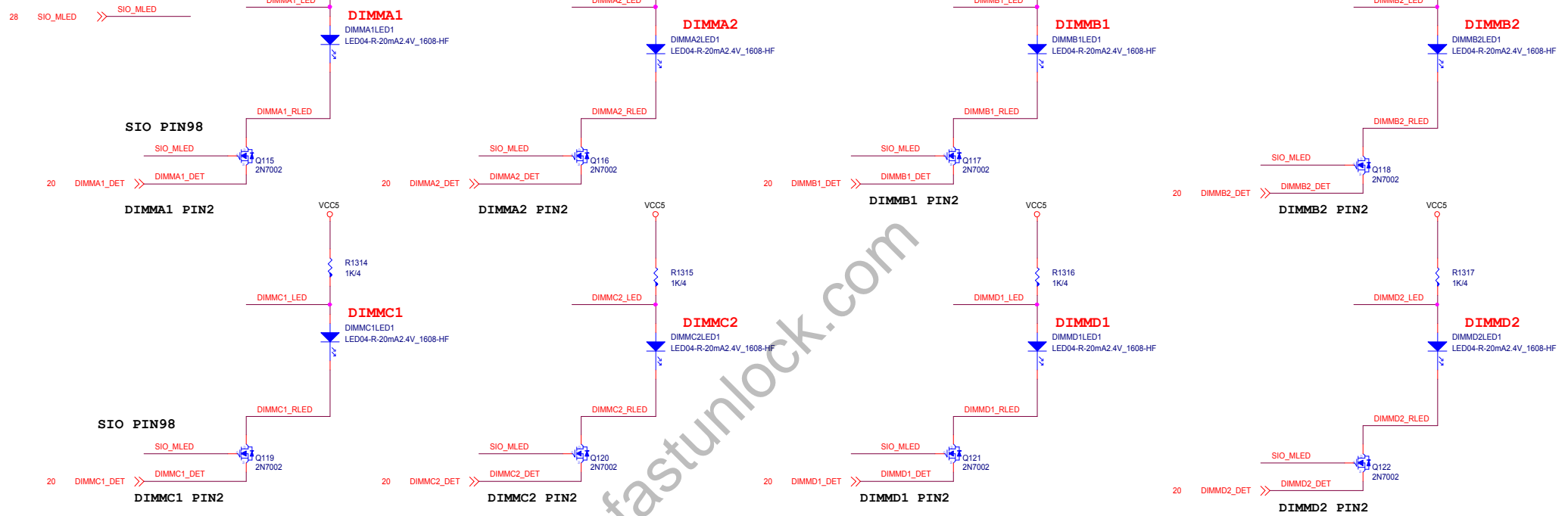
www.f0rums-fastunlock.com

www.forums-fastunlock.com

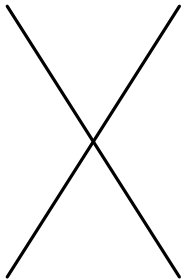
DIMM_SLOT

FORM SIO

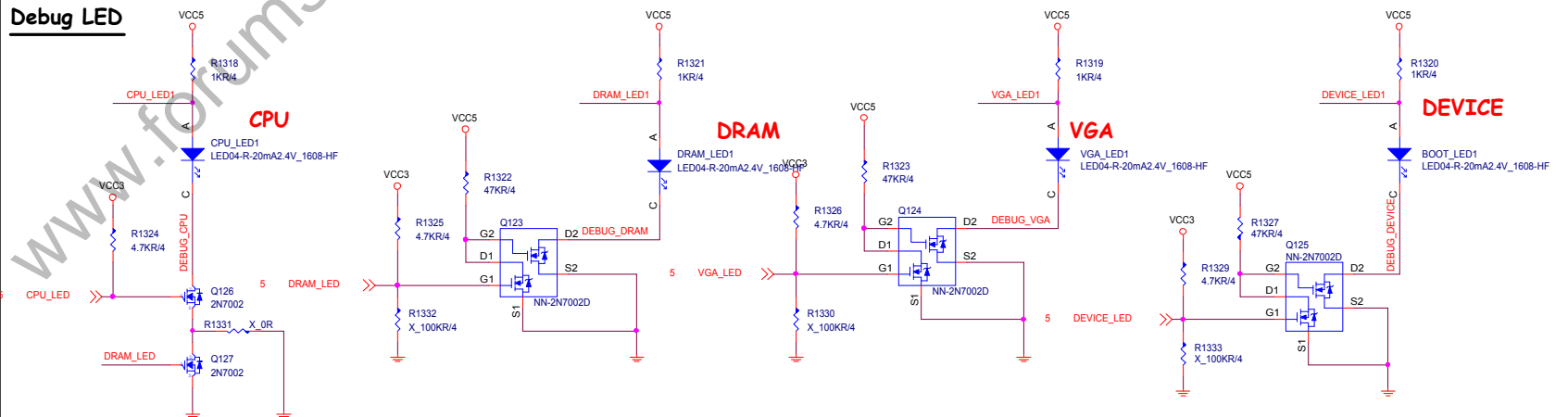
D0C-040P100-H91/D0C-040S500-E07



AMD AMP Detect LED

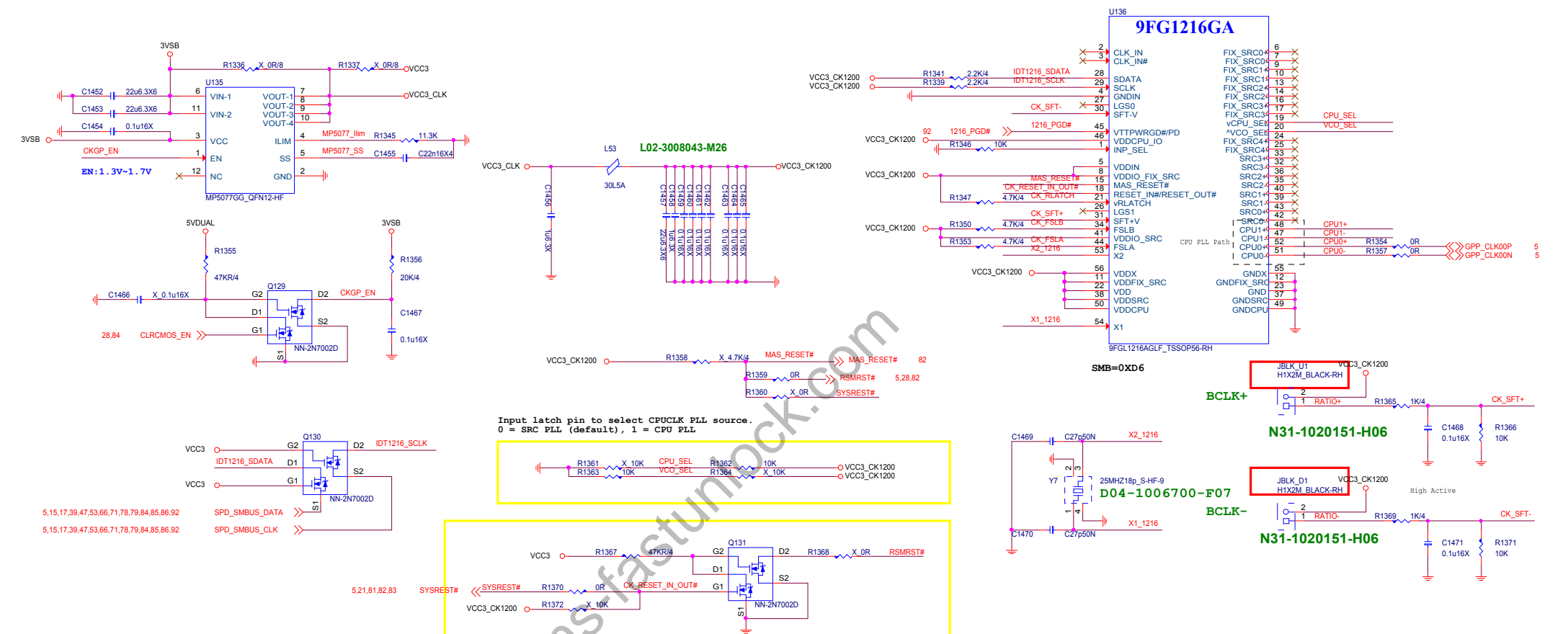


Debug LED

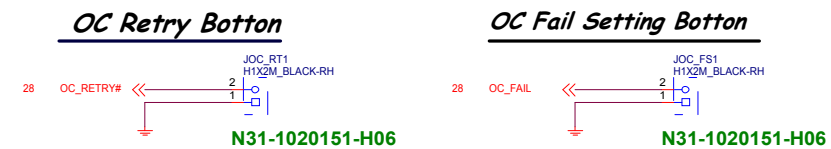
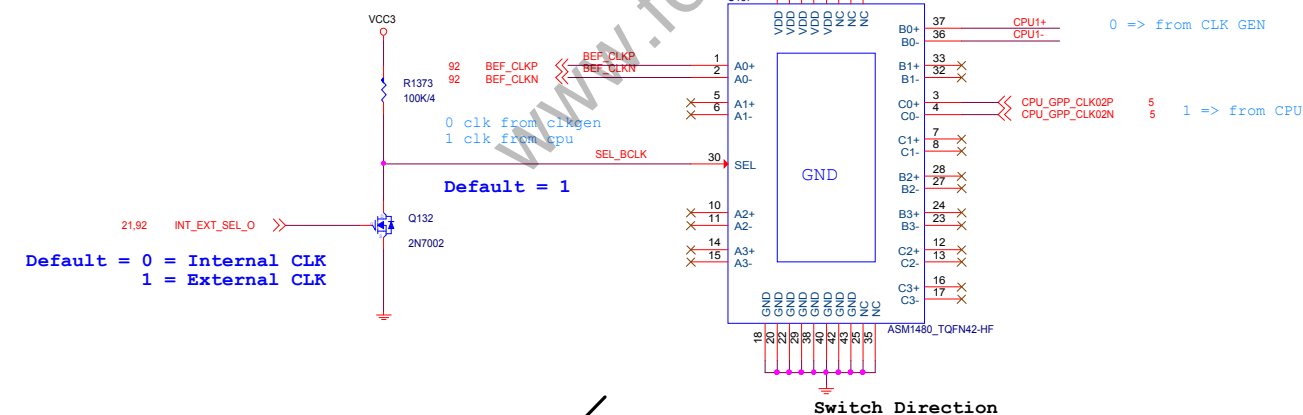


LED	GPIO	AGPIO84 0	AGPIO85 0	EGPIO84 1	EGPIO85 1
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

CLOCK GEN



CLOCK SWITCH



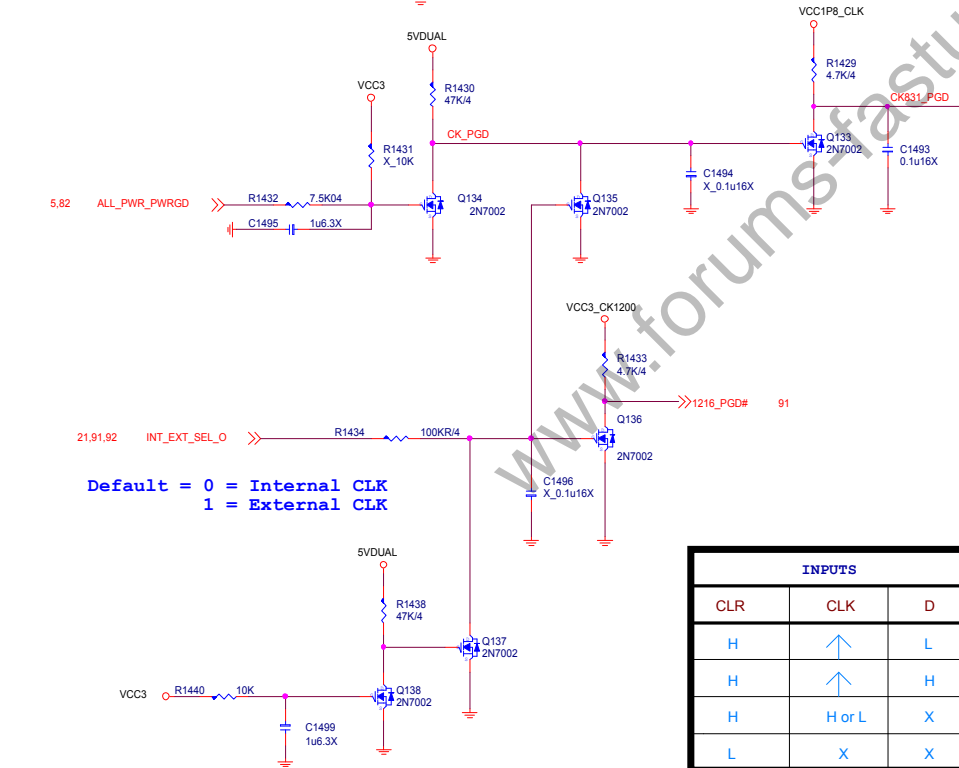
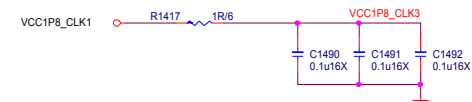
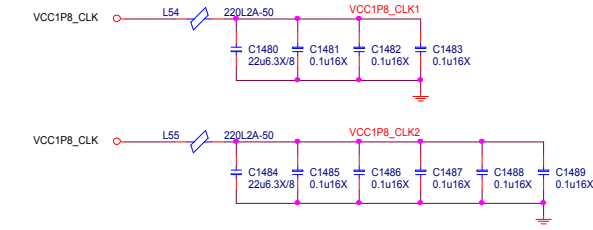
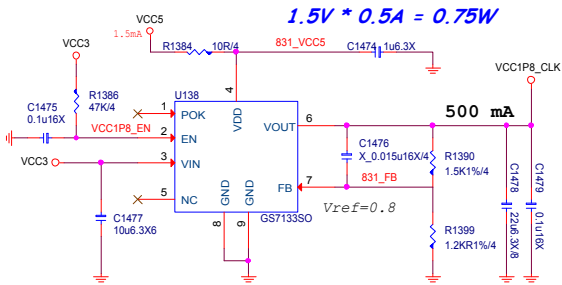
CLOCK BUFFER

5, 15, 17, 39, 47, 53, 66, 71, 78, 79, 84, 85, 86, 91
5, 15, 17, 39, 47, 53, 66, 71, 78, 79, 84, 85, 86, 91

SPD_SMBUS_CLK
SPD_SMBUS_DATA

SPD_SMBUS_CLK
SPD_SMBUS_DATA

$$1.5V * 0.5A = 0.75W$$



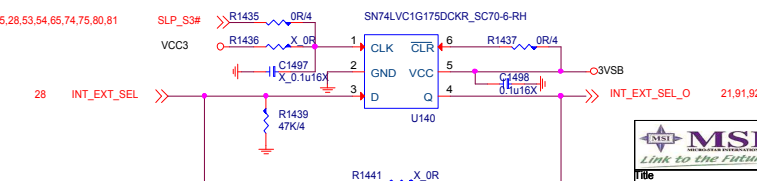
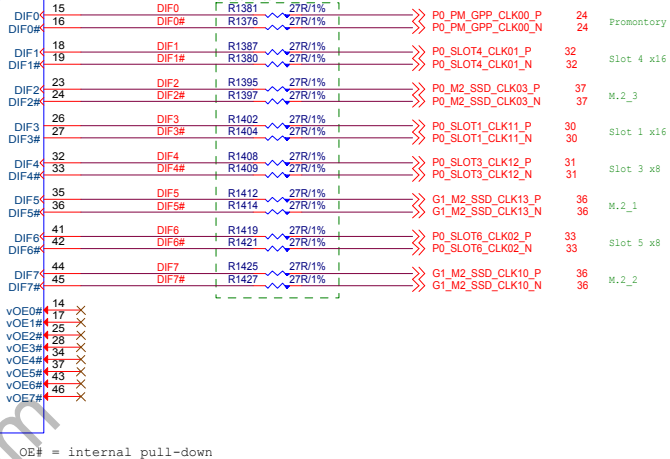
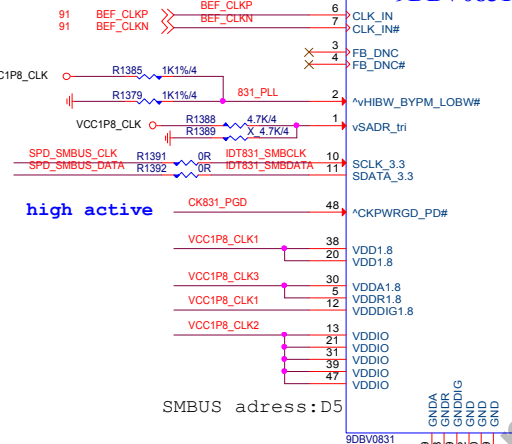
Default = 0 = Internal CLK
1 = External CLK

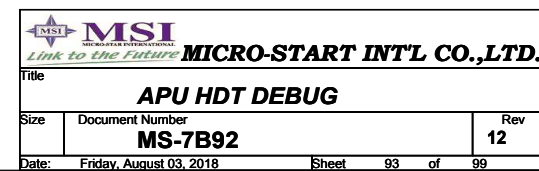
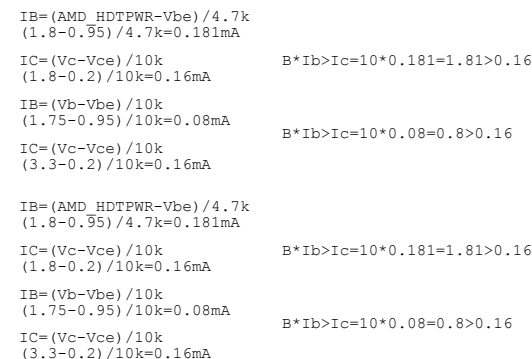
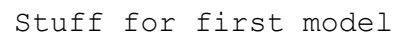
high active

SMBUS address:D5

INPUTS			OUTPUTS
CLR	CLK	D	Q
H	↑	L	L
H	↑	H	H
H	H or L	X	Qo
L	X	X	L

9DBV0831

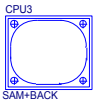
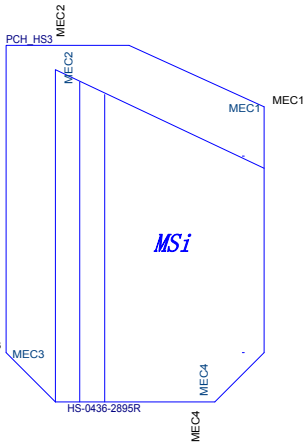
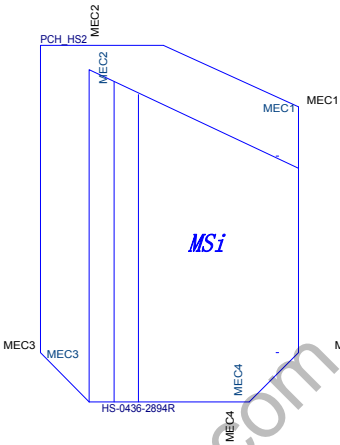
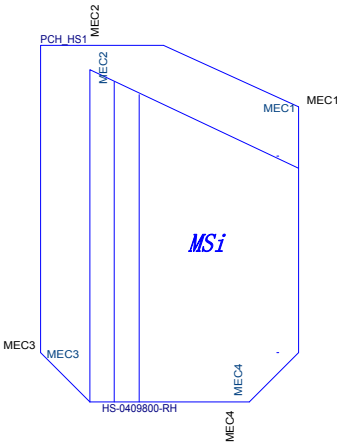
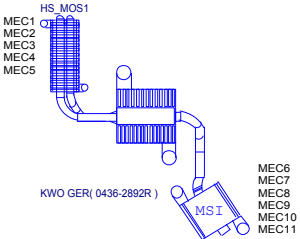




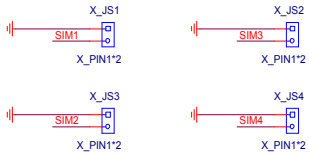
CPU HEAT SINK

PCH HEAT SINK

CPU Socket



Simulation



MANUAL PART

AMI1
AMI LABEL
G51-M1SPXXA-A09

CFOS1
Label
VIRTUAL
CFOS
Y02-MU00170-CFO

NAHIMIC1
Label
BUNDLE
NAHIMIC
Y02-MU00100-NAH

SLI1
Label
VIRTUAL
SLI
Y01-RNVIDIN-000

MKT1
Label
BUNDLE
X_MKT
G51-M1SPL82-Q13

XSPLIT1
Label
BUNDLE
X_XSPLIT
Y02-MA00401-XSP

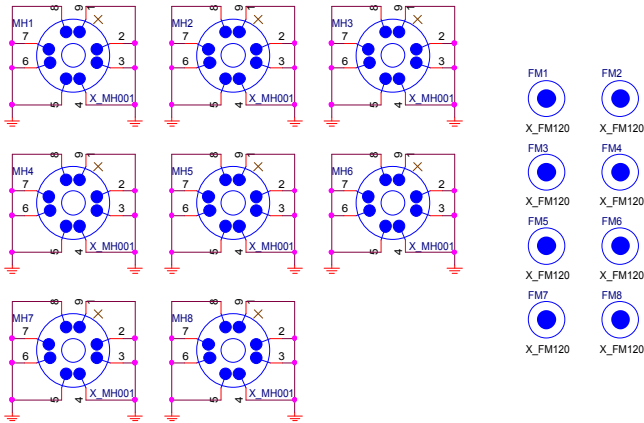
SSE1
Label
VIRTUAL
X_SSE
Y02-MA00101-SSE

BAT1_X1
BAT-CR2032-RH
D06-0100101-P01

PCB1
7B92-1.2
PD0-07B9212-G37, 精成-深圳, 0, 寶安恩斯邁廠 (MSIS)
601-7B92-020 .001 MP

PCH_HS2與PCH_HS3出BOM前要再加回來

Optics Orientation Holes



Add for EMI

